Advanced Analog Integrated Circuits

MOS Switches

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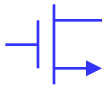
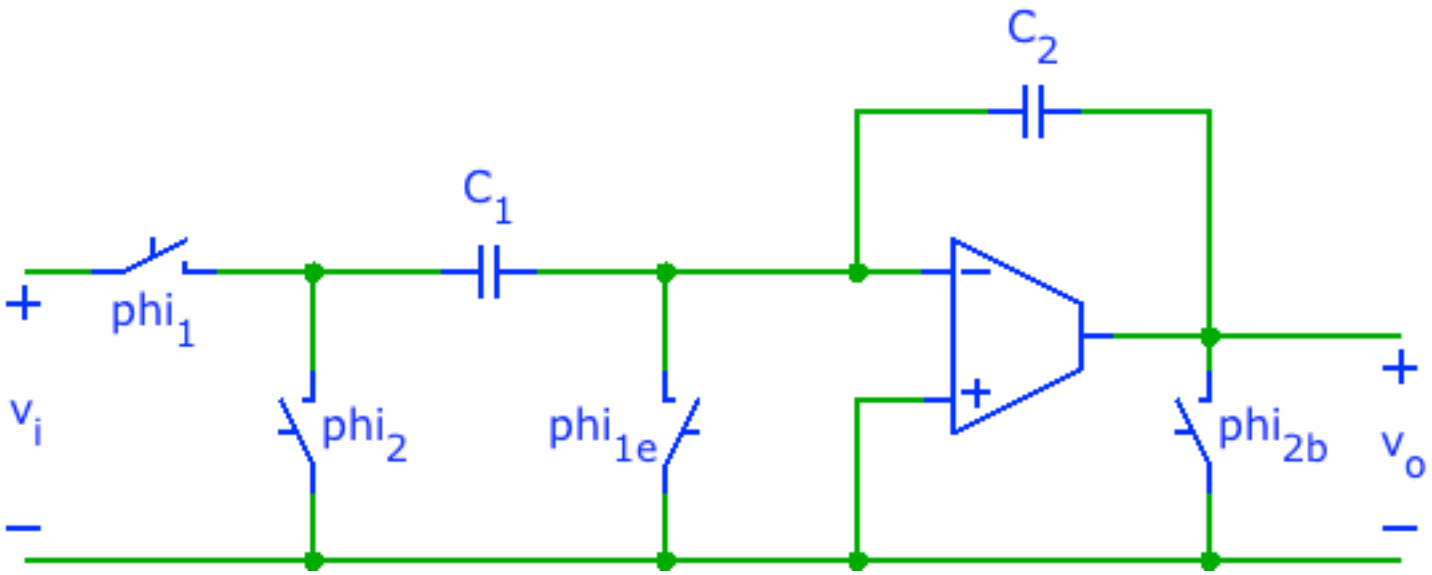
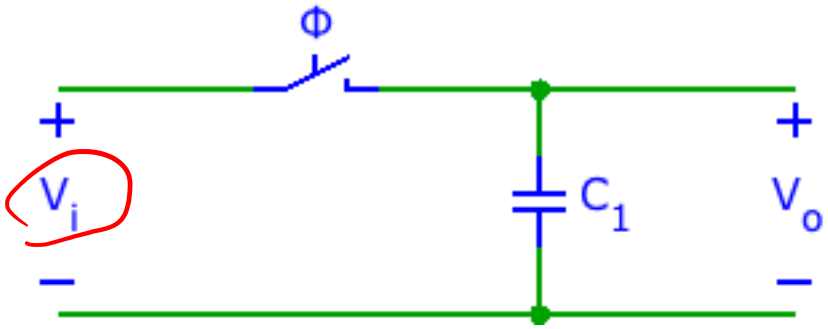
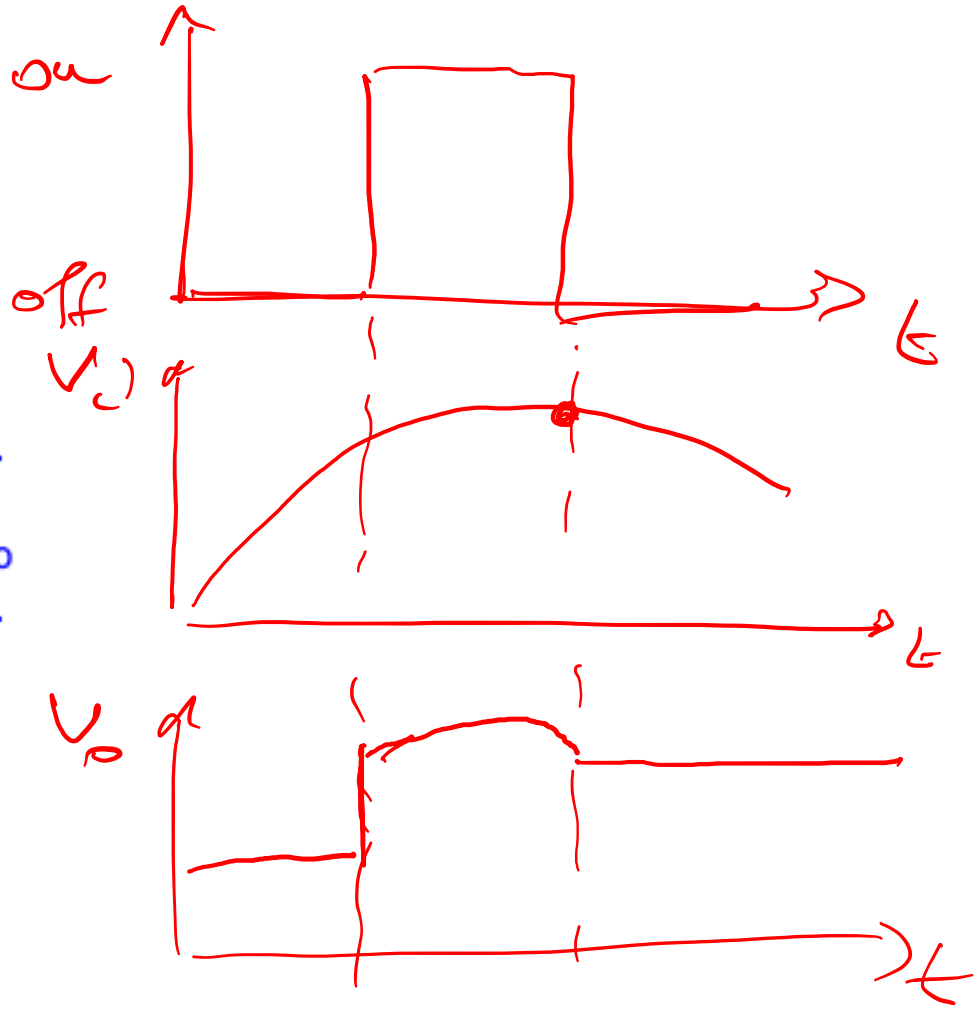


MOS Switches



Ideal Track and Hold

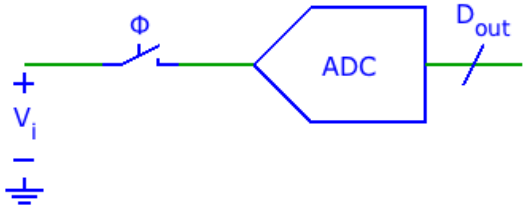


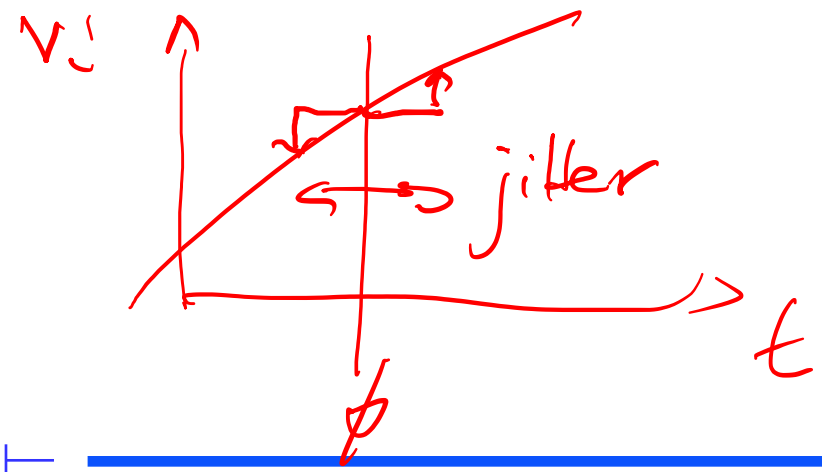


Sampling versus Charge Processing

Sampling

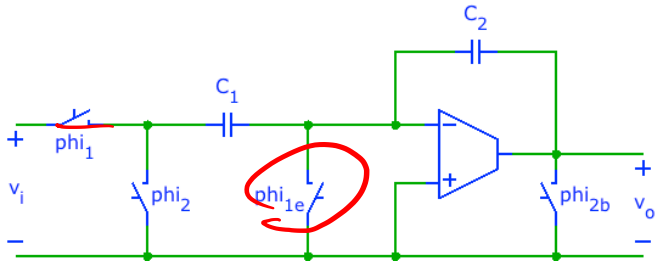
- Input varies (often rapidly)

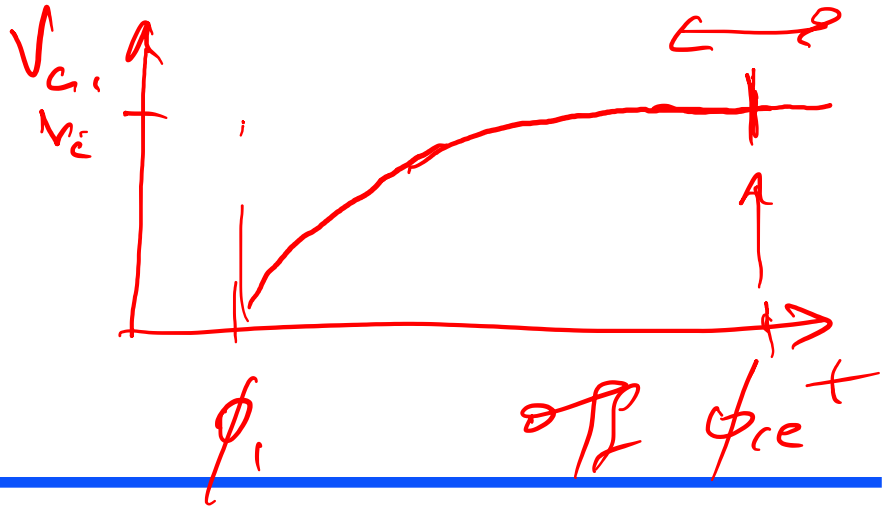




Charge Processing (SC)

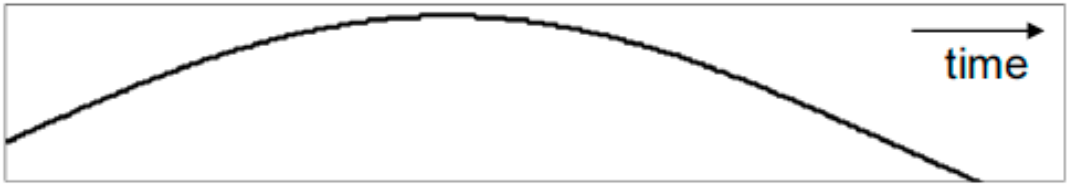
- Input ~constant





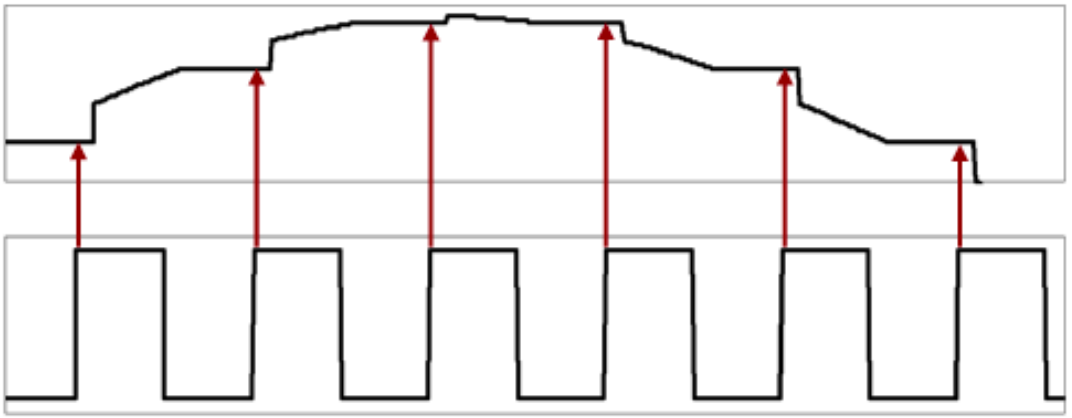
Signal Nomenclature

Continuous Time Signal

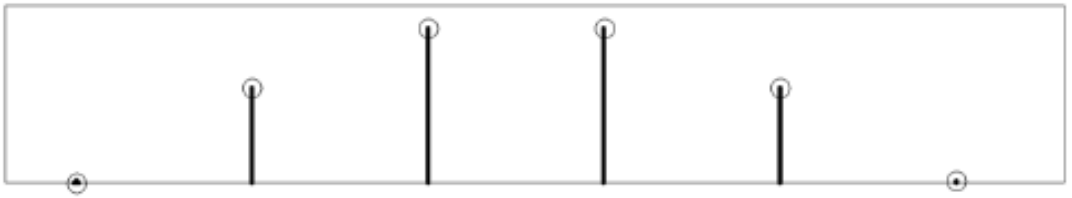


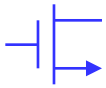
T/H Signal
("Sampled Data Signal")

Clock

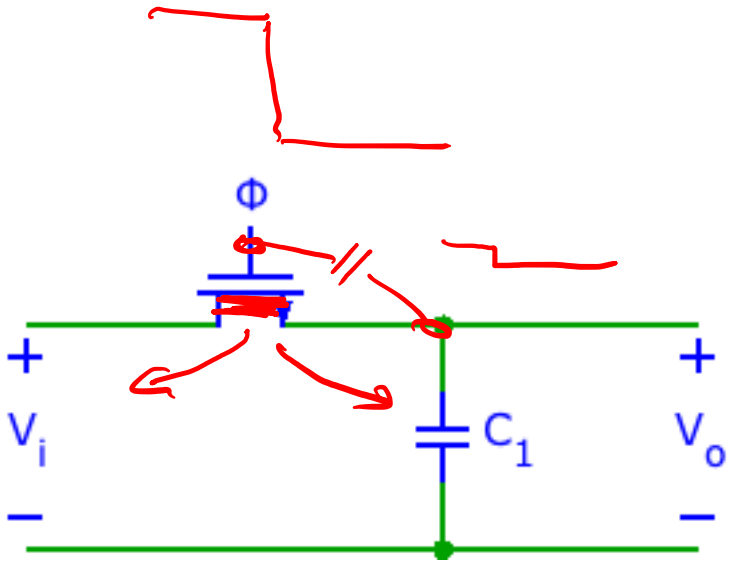


Discrete Time Signal

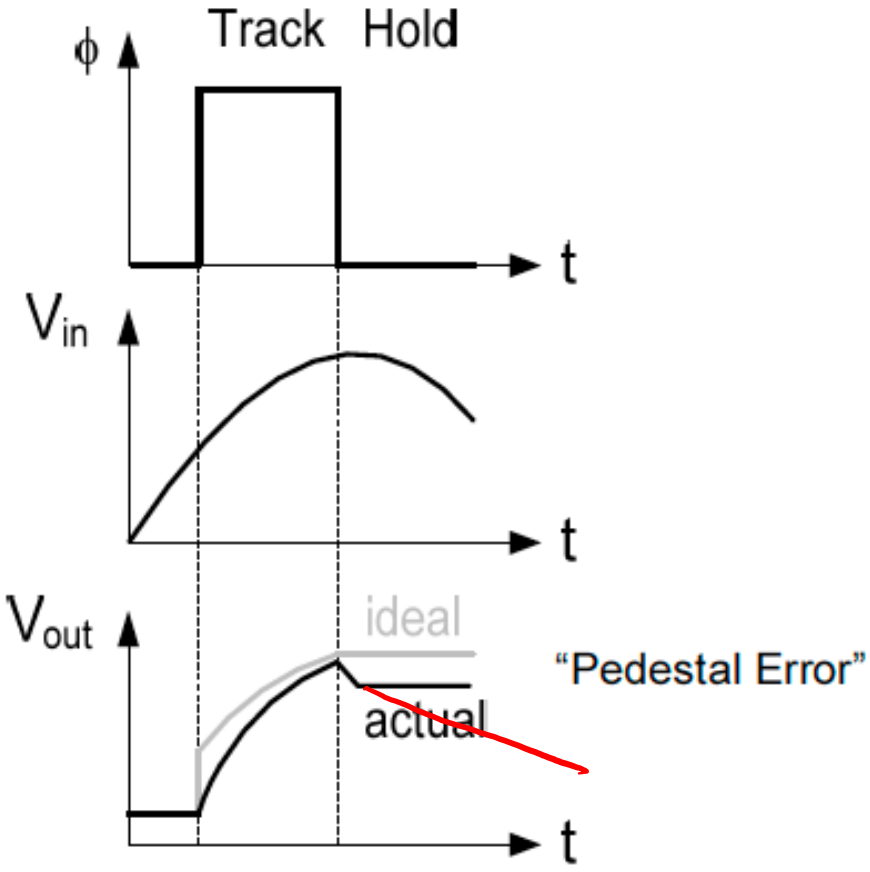




MOS Sample & Hold (Track & Hold)



(simplest realization)



Advanced Analog Integrated Circuits

Switch Nonidealities

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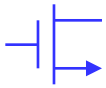
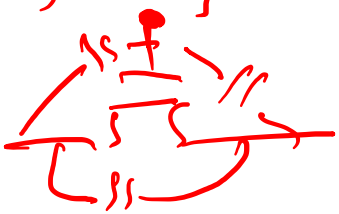
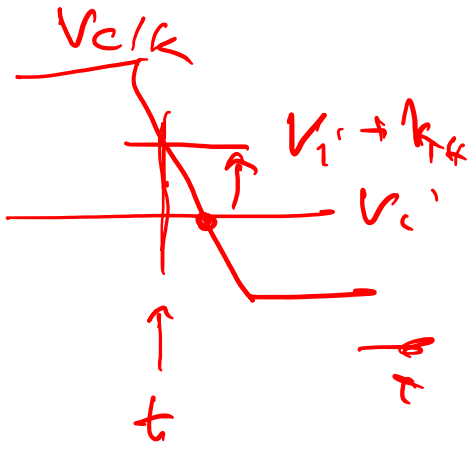


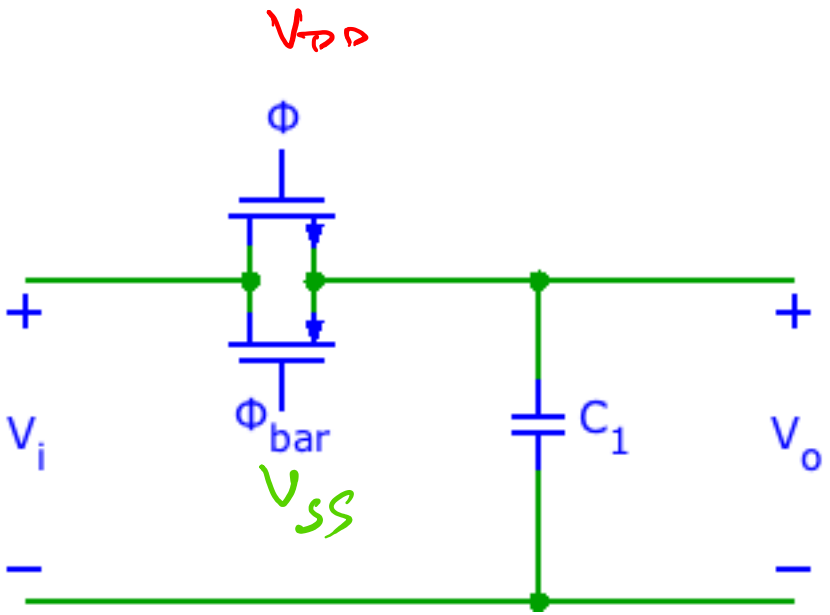
Nonidealities

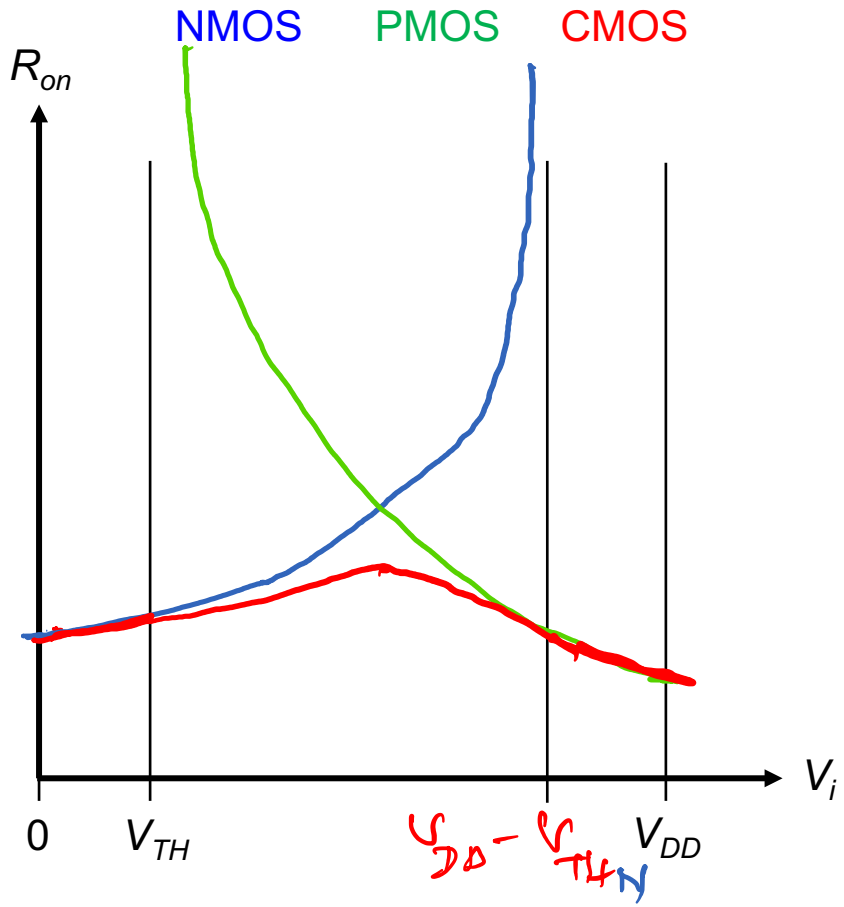
- R_{on} finite, tracking BW
- Tracking nonlinearity
- Signal dep sampling time
- Thermal noise
- Clock jitter
- Hold feed-through
- Leakage
- Charge injection



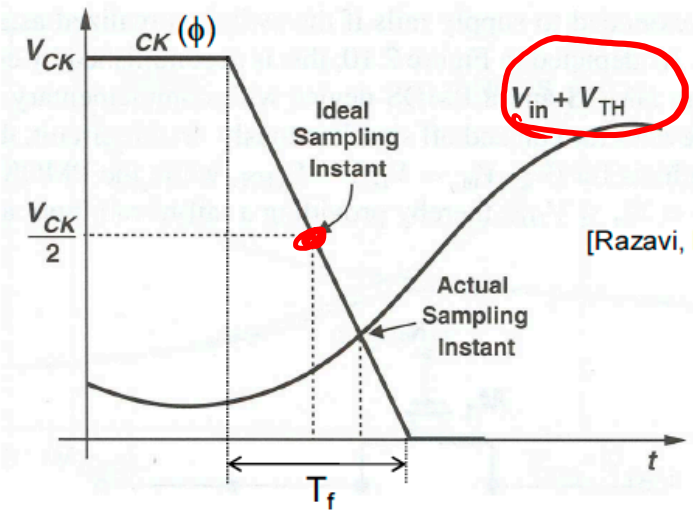


Switch on-resistance



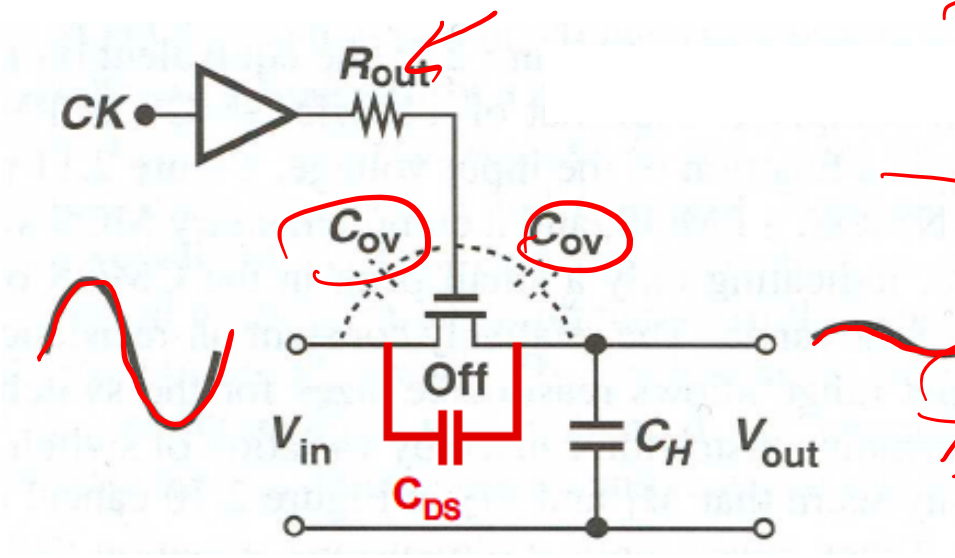


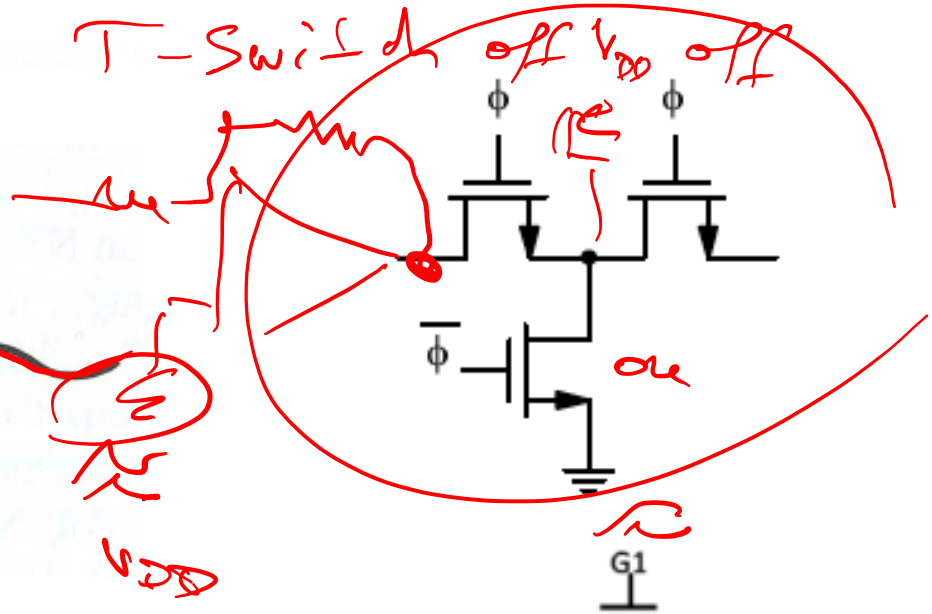
Signal Dependent on-resistance

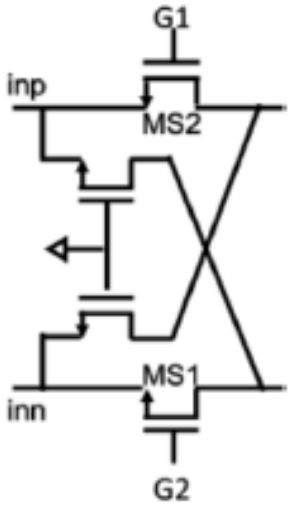


[Razavi, Data Conversion System Design, p.17]

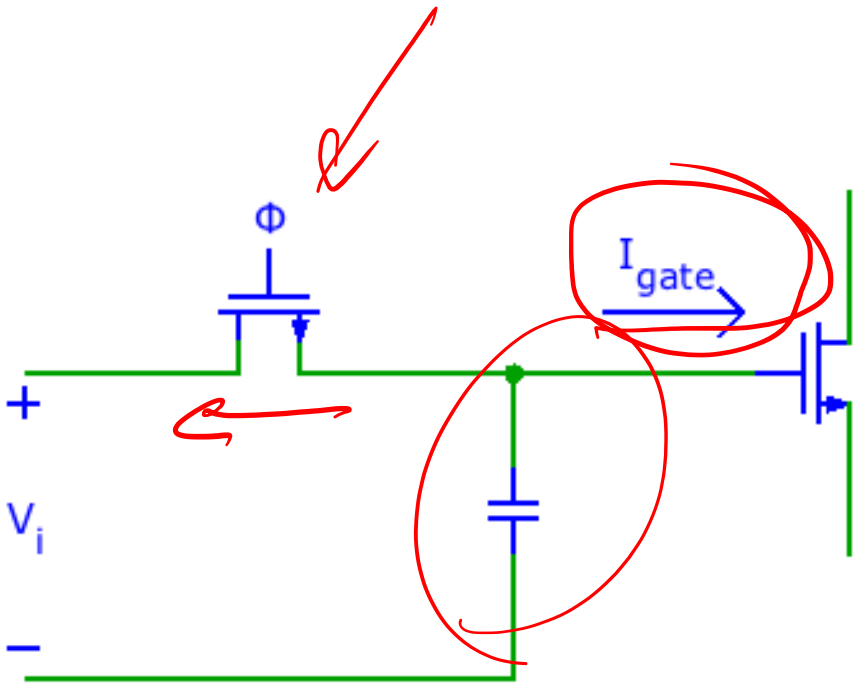
Hold-Mode Feedthrough

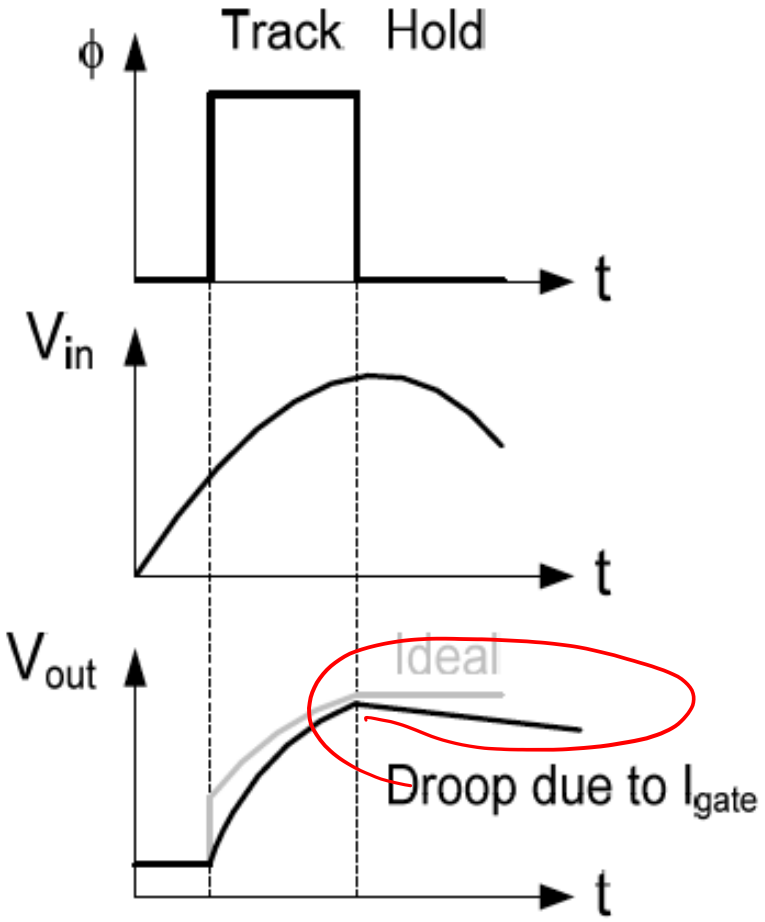




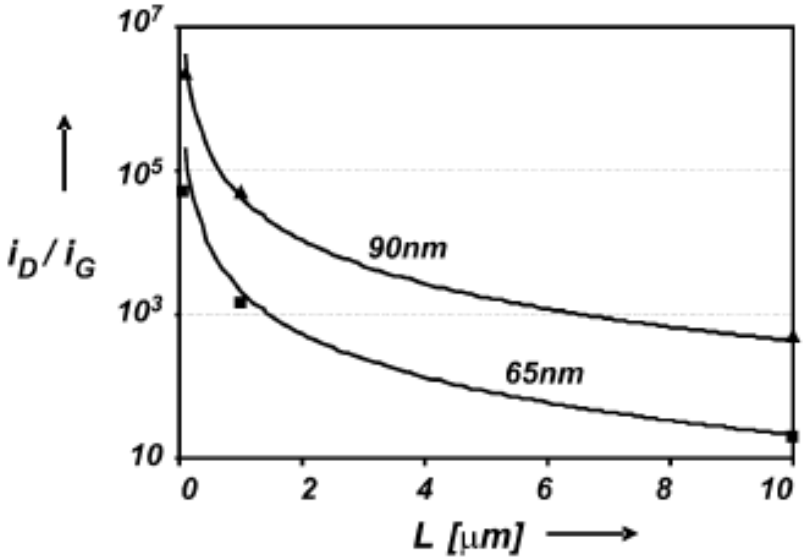


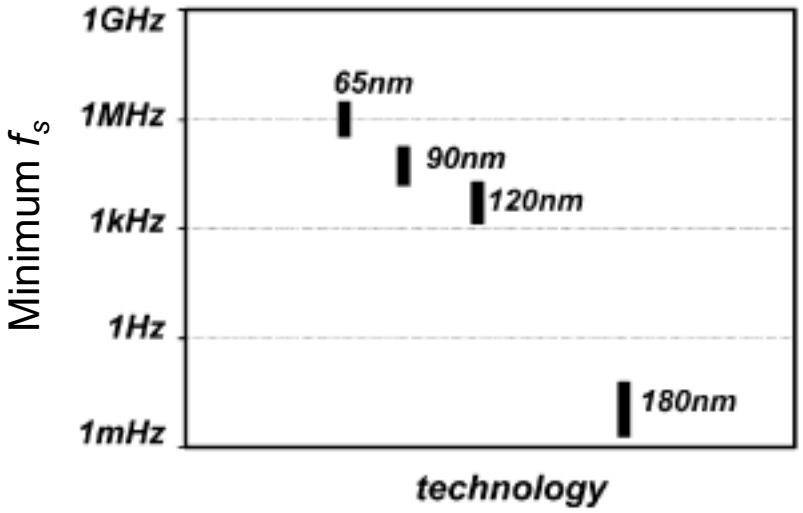
Hold-Mode Leakage





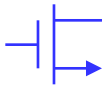
Gate Leakage



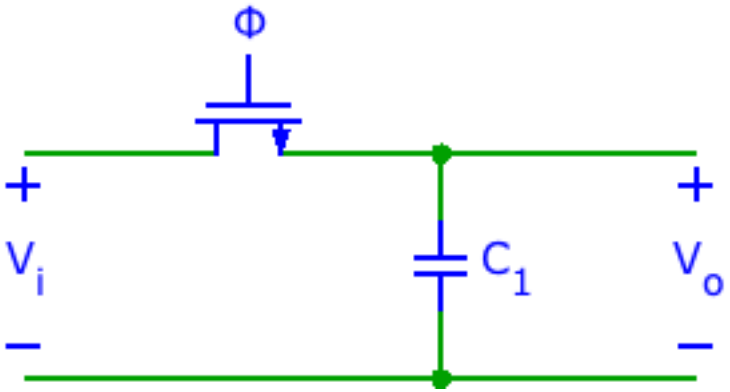


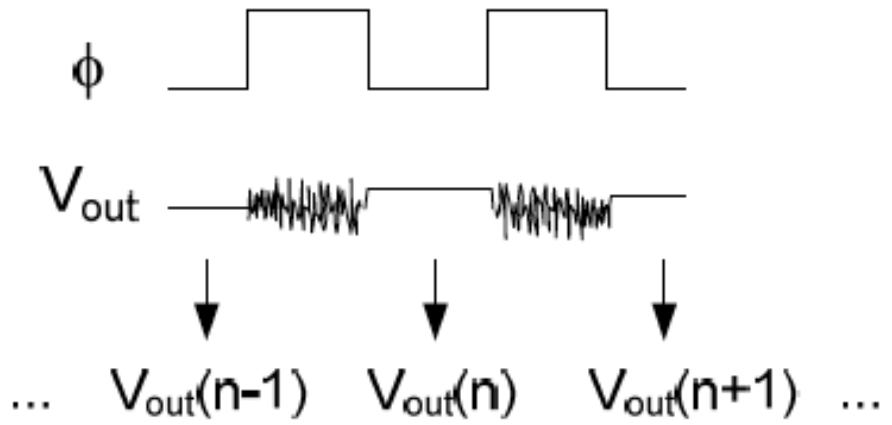
- 65nm CMOS: ~ 1V/ms droop
  - Addressed in sub-65nm technologies with high-k dielectrics

Ref: A. Annema et al, “Analog circuits in ultra-deep-submicron CMOS,” IEEE JSSC, Jan. 2005, pp. 132-43.

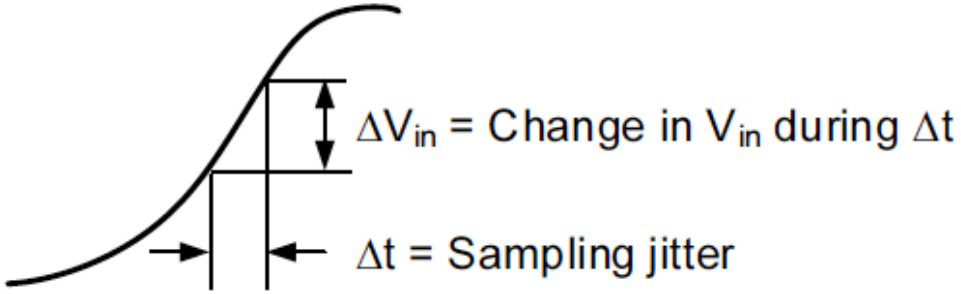


Thermal Noise





Clock Jitter



$$\Delta V_{in} \cong \frac{dV_{in}}{dt} \cdot \Delta t$$

Advanced Analog Integrated Circuits

Charge Injection and Clock Feedthrough

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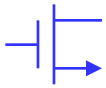
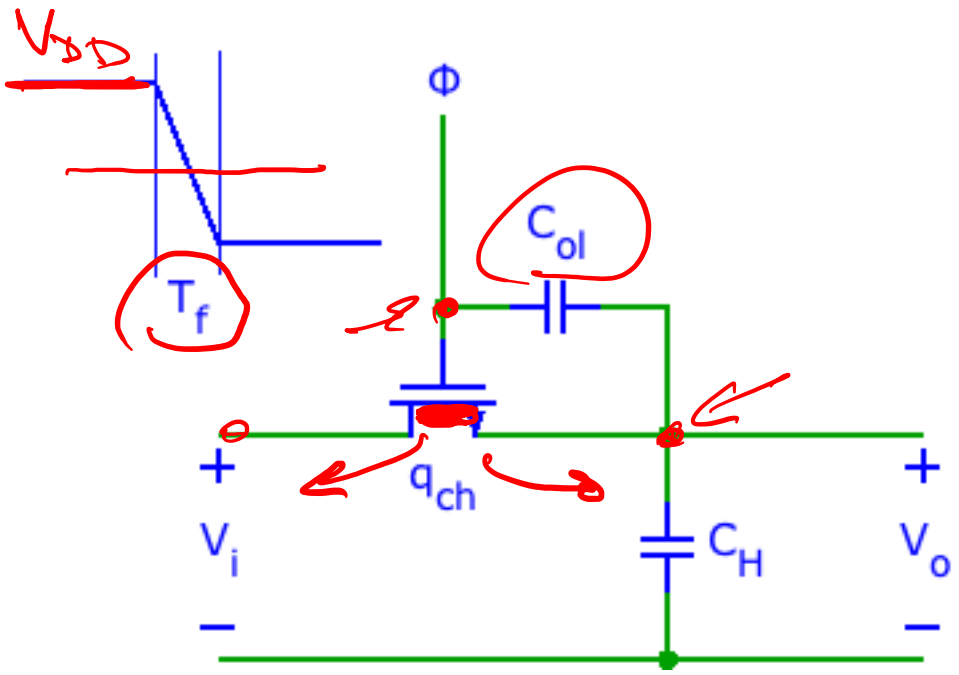
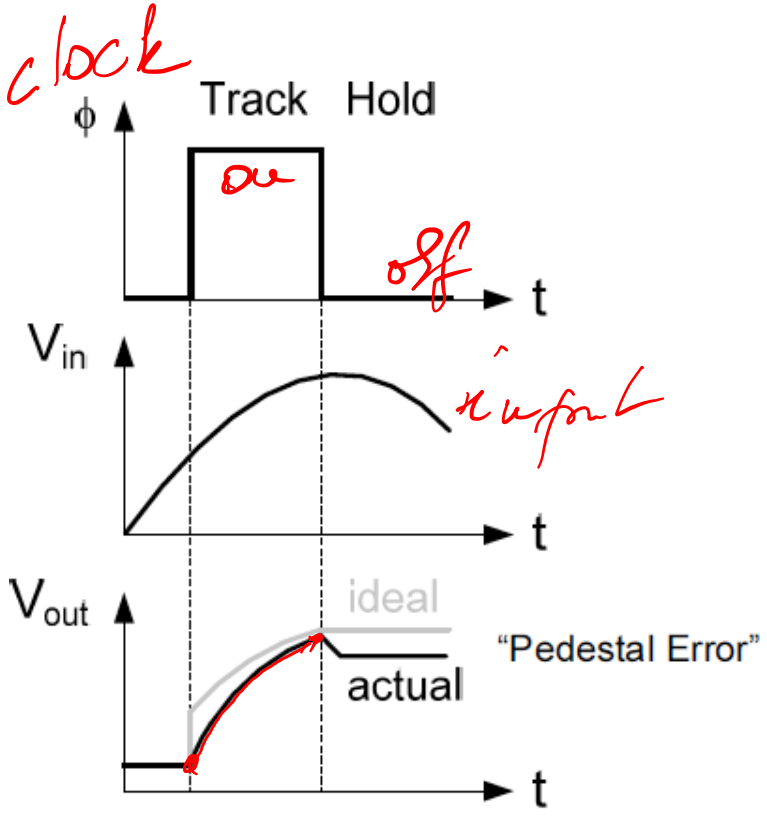


Charge Injection and Clock Feedthrough

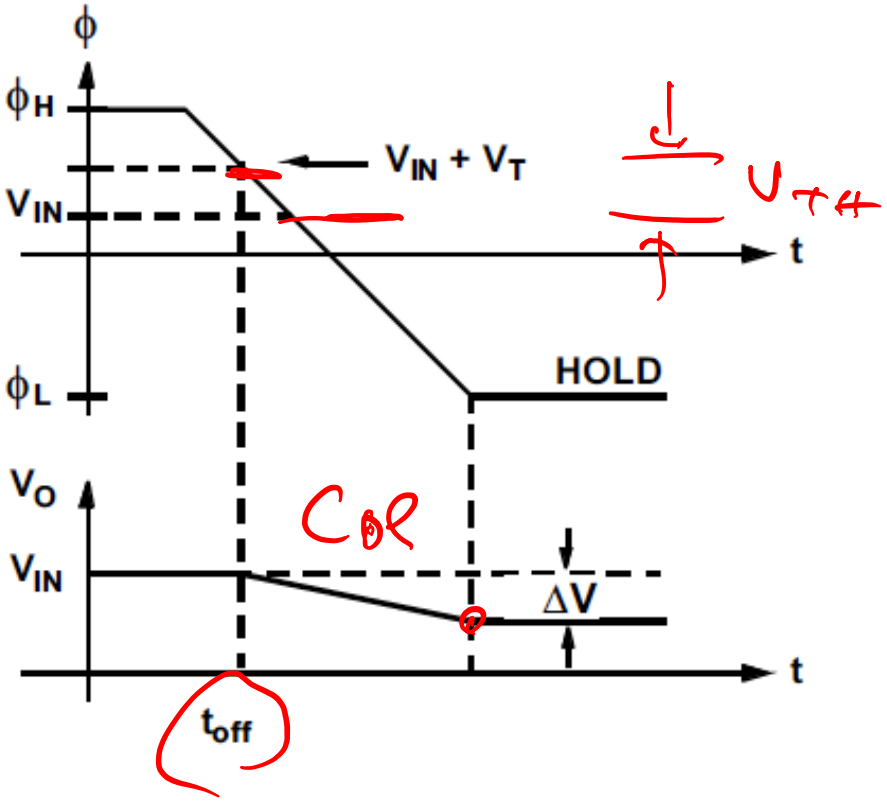




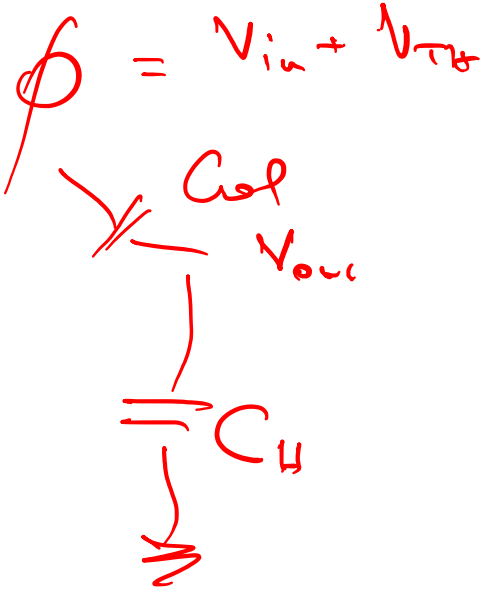
Extreme Cases:

- slow $T_f \gg \tau$
- fast $T_f \sim \tau$

Slow Gating



Slow Gating Model



error

$$V_{out} = V_{in} - \Delta V_{out}$$

$$= V_{in} - \frac{C_{ol}}{C_{ol}+C_H} \cdot (V_{in} - V_{TH} - \phi_L)$$

(ϕ_L = V_{SS})

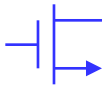
$$= V_{in}(1+\varepsilon) + V_{os}$$

$$\varepsilon = -\frac{C_{ol}}{C_{ol}+C_H} \qquad V_{os} = \varepsilon \cdot (V_{TH} + \phi_L)$$

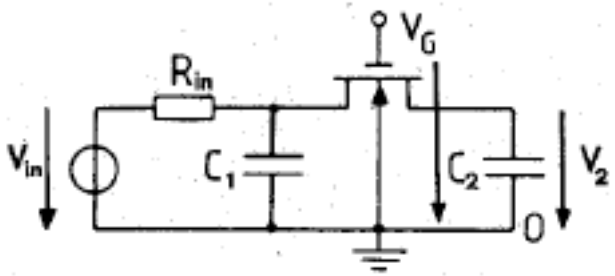
E.g. $C_H = 1pF$ $\phi_L = 0V$ $V_{TH} = .45V$ $C_{ol} = .1fF$

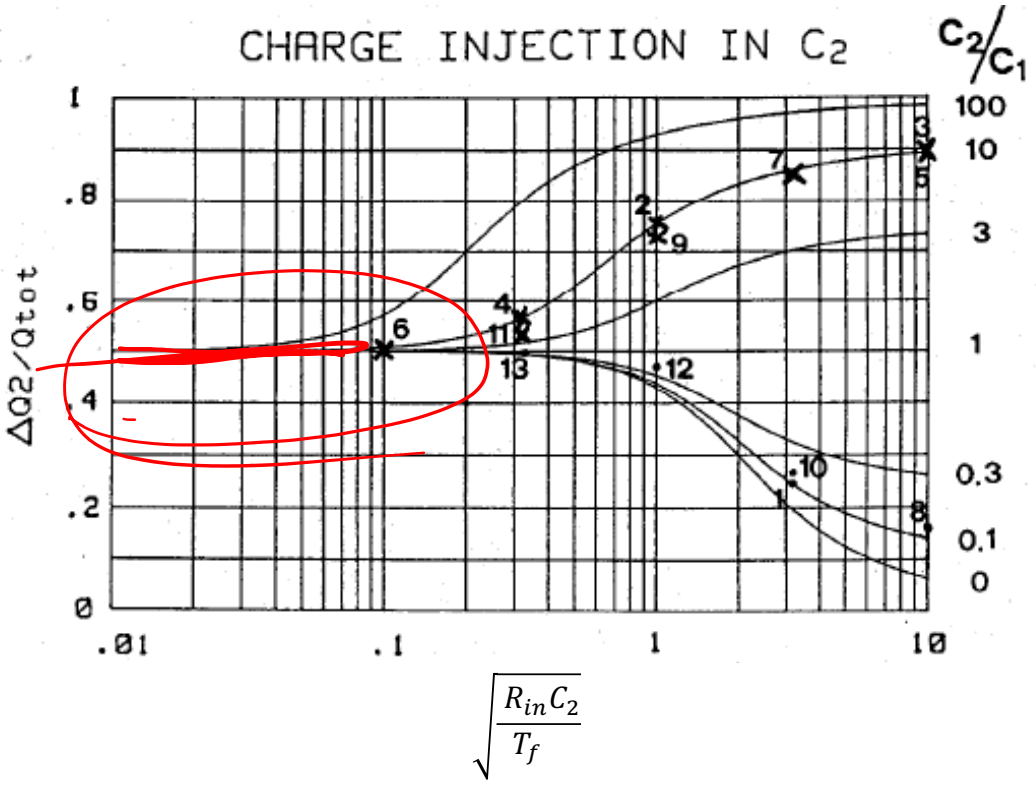
$\varepsilon = -0.2\%$ $V_{os} = -0.9mV$ $C_{ol} = 2fF$

Fast Gating



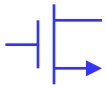
Charge Split Ratio α



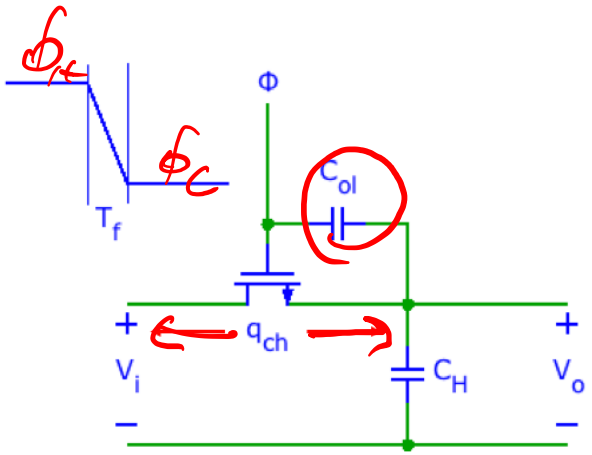


Ref: G. Wegemann et al, “Charge injection in analog MOS switches,” IEEE JSSC, June 1987, pp. 1091-7.

Slow Switching or Fast Switching?



Fast Gating Model



$$V_{on} = V_{in} - \frac{C_{ol}}{C_{ol}+C_H}(\phi_H - \phi_L) + \frac{Q_{CH}}{2C_H}$$

$$Q_{CH} = -WLC_{ox}(\phi_H - V_{in} - V_{TH})$$

$$\xi = \frac{WLC_{ox}}{2C_H}$$

$$V_{os} = -\frac{C_{ol}}{C_{ol}+C_H}\cdot(\phi_H - \phi_L) - \frac{1}{2}\frac{WLC_{ox}}{C_H}\cdot(\phi - V_{TH})$$

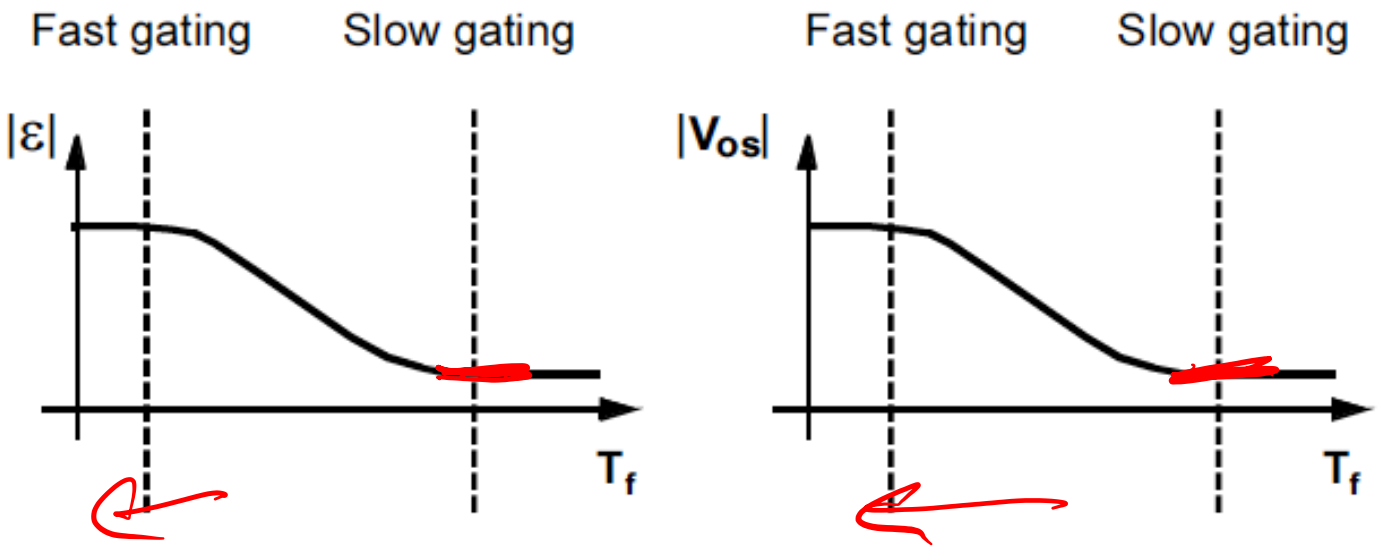
E.g. $C_H = 1pF$

$\phi_H - \phi_L = 1.8V$ $V_{TH} = .45V$ $W = 2\mu m$ $L = 180nm$

$LC_{ox} = 2fF/\mu m^2$

$\xi = 2\%$ $V_{os} = -30.6mV$

Fast → Slow Gating Errors



Technology Scaling

$$\Delta V \propto \frac{Q_{CH}}{C_H} \propto \frac{C_{GS}}{C_H} \propto \frac{1}{C_H \cdot f_T}$$

$$f_S \propto \frac{1}{R_{ON} \cdot C_H} \propto \frac{1}{L \cdot C_H}$$

$$\left.\begin{array}{l} \Delta V \propto f_T \cdot L \\ f_S \end{array}\right.$$

Advanced Analog Integrated Circuits

Mitigating Charge Injection Error

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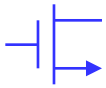


Mitigating Charge Injection Error

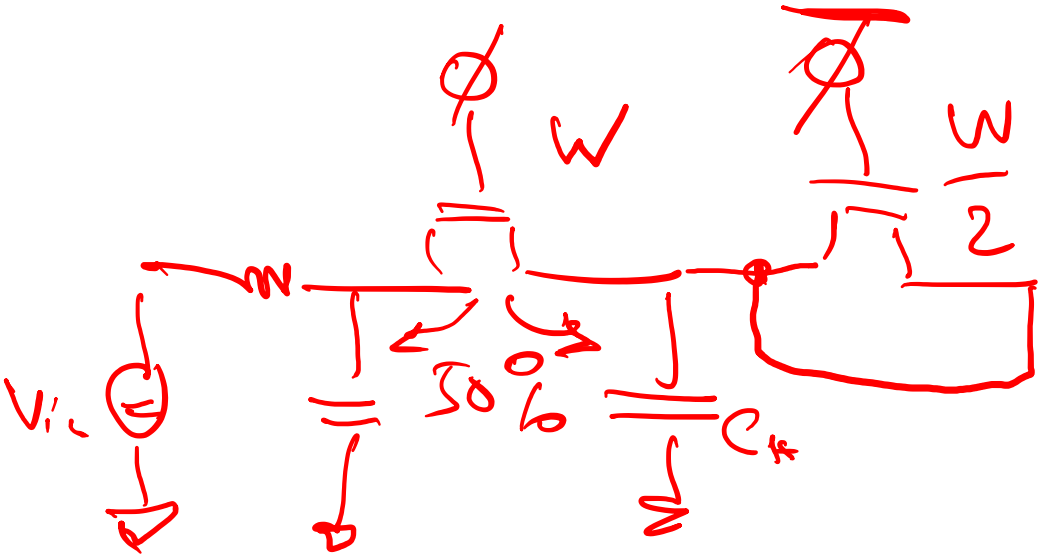
1) Charge Cancellation

2) CMOS switch

3) Diff Sampling ⇐ 

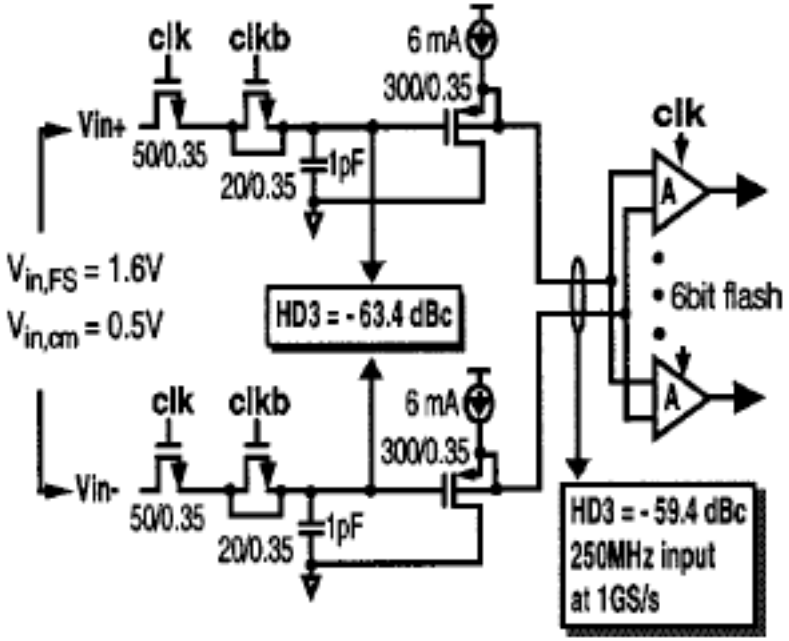
⇒ make charge inj. a Common mode signal

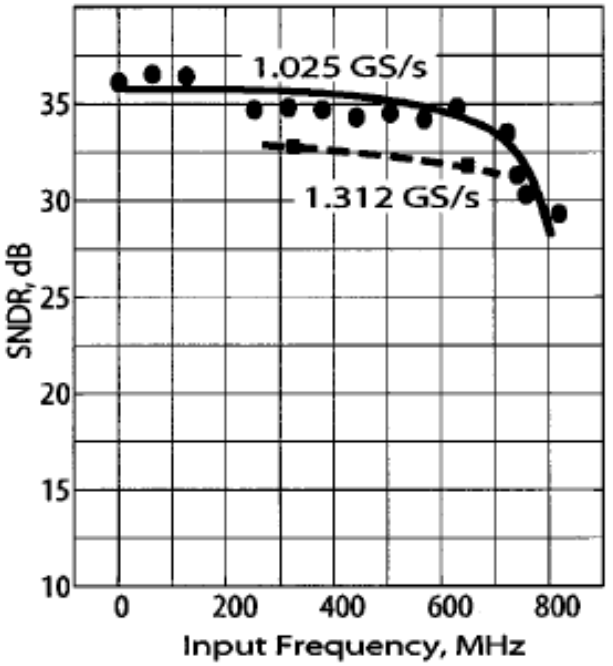
Charge Cancellation



Ref: Ch. Eigenberger et al, “Dummy Transistor compensation of analog MOS switches,” JSSC Aug 1989, pp. 1140-6.

Charge Cancellation Example

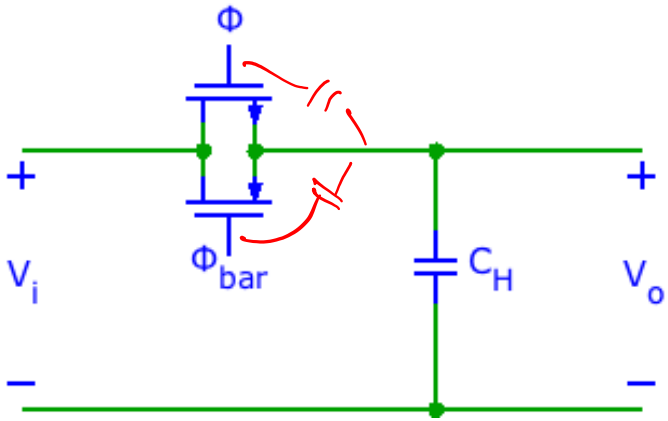




- ~ 6-Bit accuracy

Ref: M. Choi et al, "A 6-b 1.3-Gsample/s A/D converter in 0.35mm CMOS." JSSC Dec 2001, pp. 1847-58.

CMOS Switch



$$Q_{ch,n} = -W_n L_n C_{ox}\left(\phi_t - V_{in} - V_{TN}\right)$$

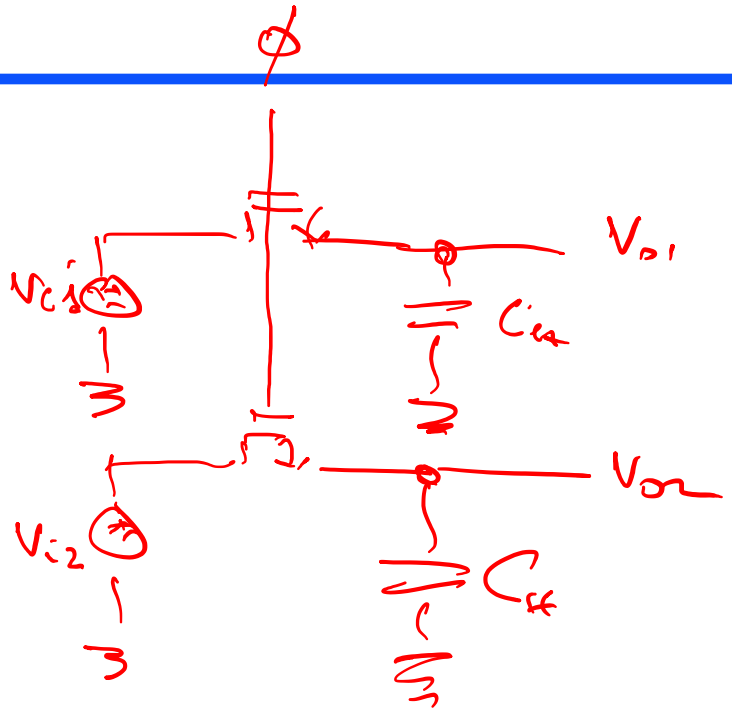
$$Q_{ch,p} = +W_p L_p C_{ox}\left(-\phi_t + V_{in} - |V_{TP}|\right)$$

- fast gates, 50/50 split:

$$\Delta V \approx \frac{C_{ox}}{C_H}\left(V_{in} - \frac{\phi_t - \phi_t}{2} + \frac{V_{TN} - |V_{TP}|}{2}\right)$$

BAD

Differential Sampling



$$V_{o1} = (1+\varepsilon_1)V_{i1} + V_{os1}$$

$$V_{o2} = (1+\varepsilon_2)V_{i2} + V_{os2}$$

$$V_{od} = \left(1 + \frac{\varepsilon_1 + \varepsilon_2}{2}\right) V_{id}$$

$$V_{oc} = (\quad\quad) V_{ic} + \frac{V_{os1} + V_{os2}}{2}$$

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Clock Bootstrapping

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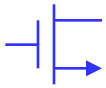
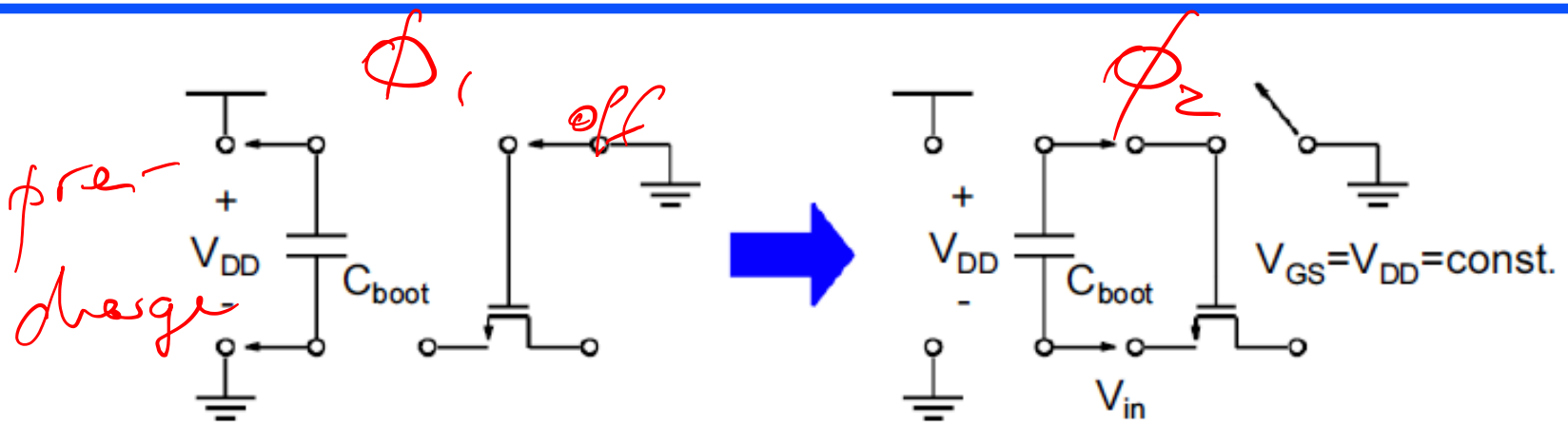
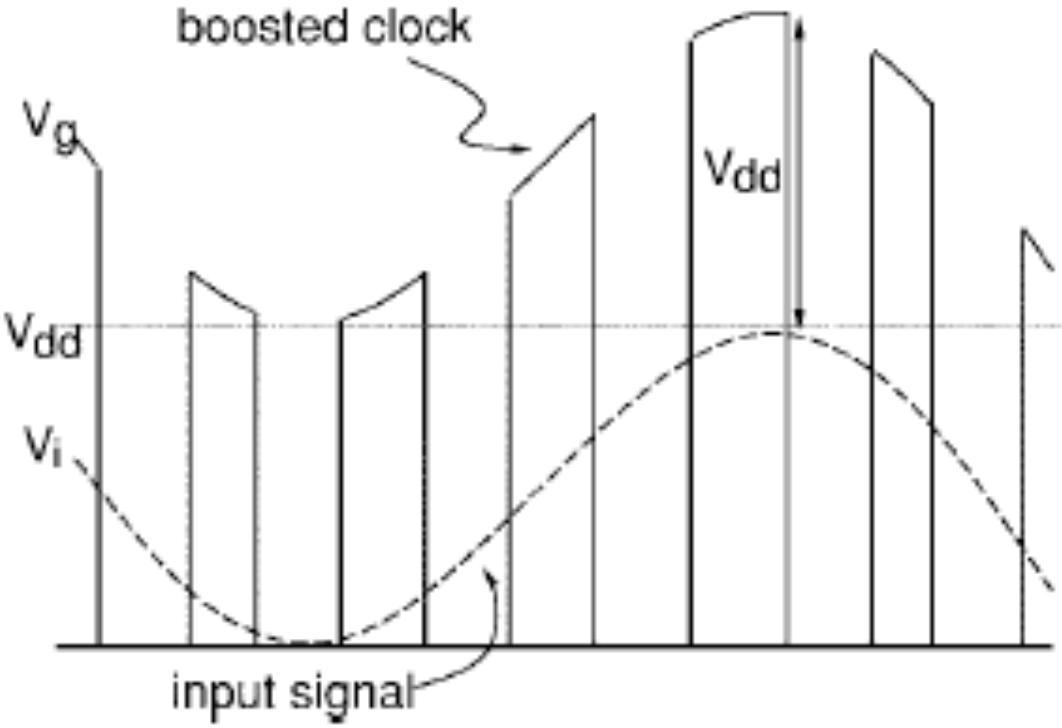


Clock Bootstrapping

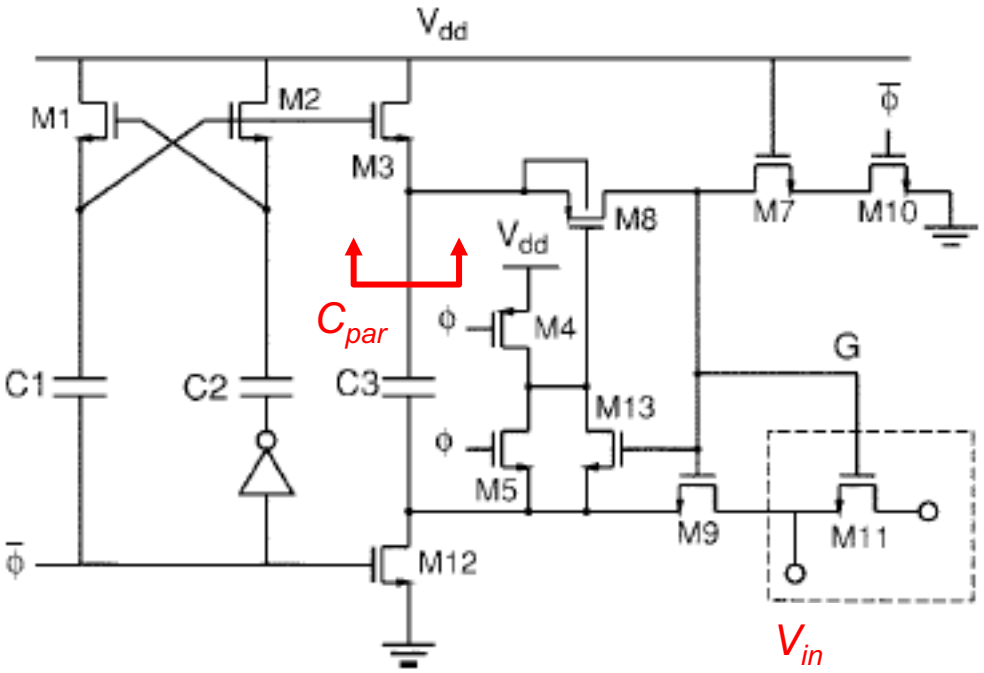


A. Abo, "Design for Reliability of Low-voltage, Switched-capacitor Circuits," PhD Thesis, UC Berkeley, 1999.

Input and Clock Waveforms



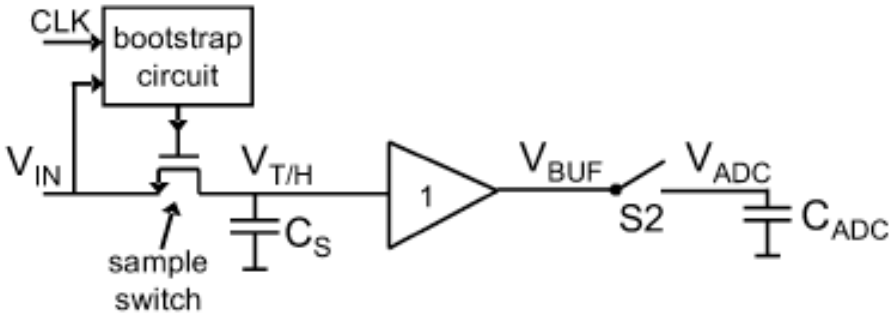
Booster Circuit

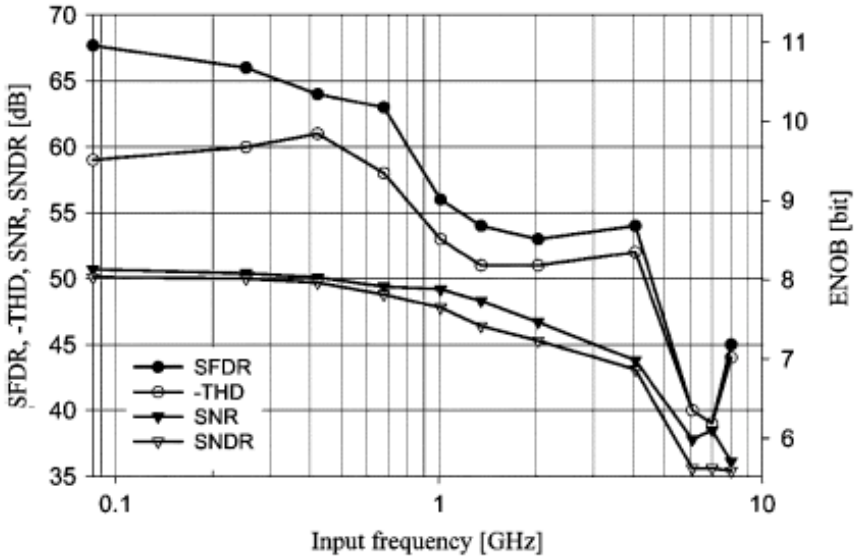


$$R_{on} \cong \frac{1}{\mu_n C_{ox} \frac{W}{L}\left\{\frac{C_3}{C_3 + C_{par}} V_{DD} - \frac{C_{par}}{C_3 + C_{par}} V_{in} - V_{TN}(V_{in})\right\}}$$

(square law model)

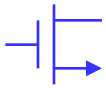
Booster Performance Example





- Good to ~ 10 Bits

Ref: S. Louwsma et al, "A 1.35 GS/s, 10 b, 175 mW time-interleaved AD converter in 0.13 um CMOS", JSSC April 2008, pp. 778-86.



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Bottom Plate Sampling

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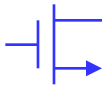
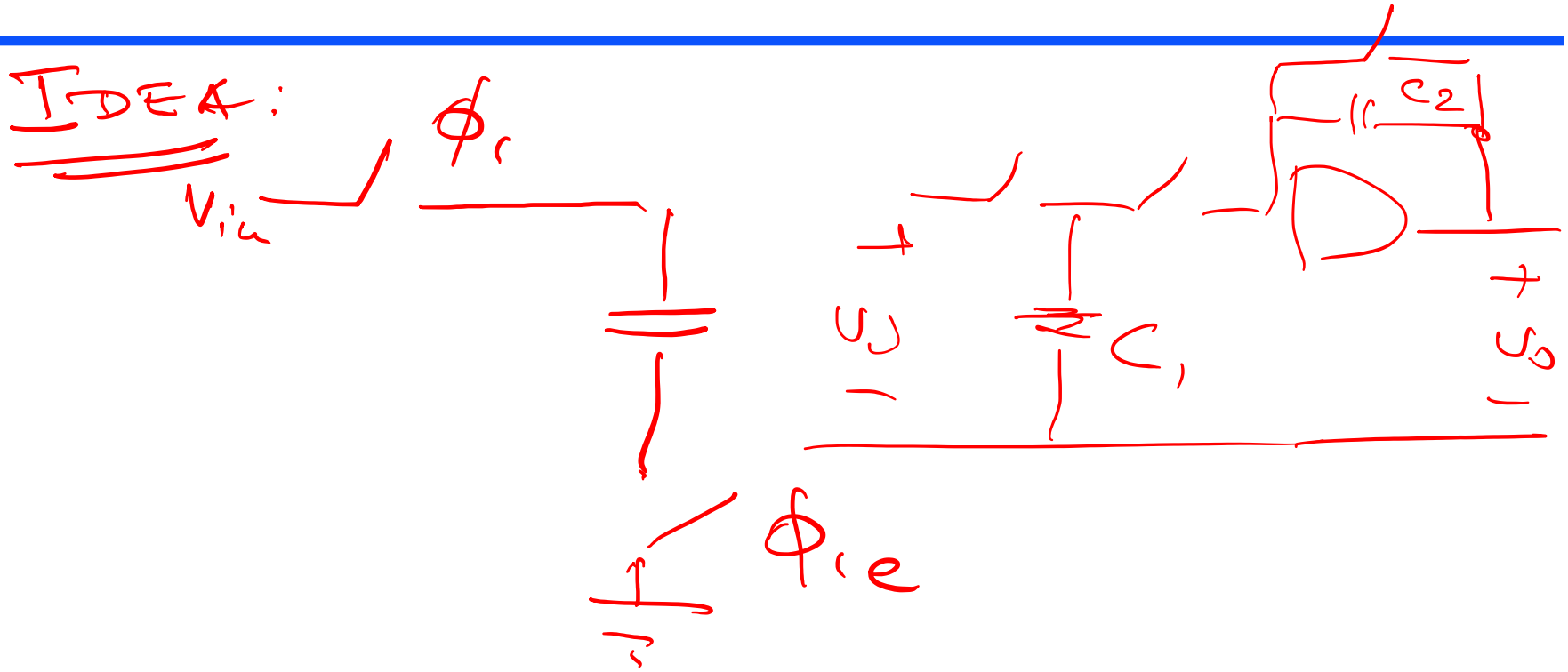
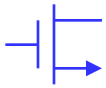


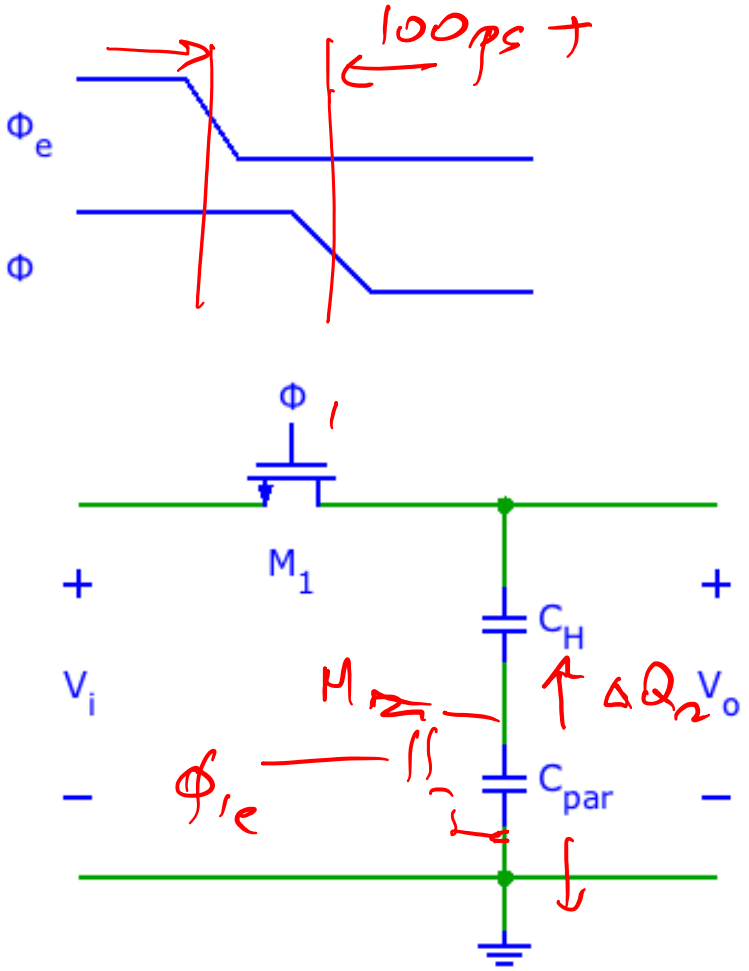
Bottom Plate Sampling



- References
  - D. G. Haigh and B. Singh, “A switching scheme for SC filters which reduces the effect of parasitic capacitances associated with switch control terminals,” ISCAS 1983, pp. 586-9.
  - K.-L. Lee and R. G. Meyer, “Low-distortion switched-capacitor filter design techniques,” IEEE JSSC, Dec 1985, pp. 1103-13.



1) Sample

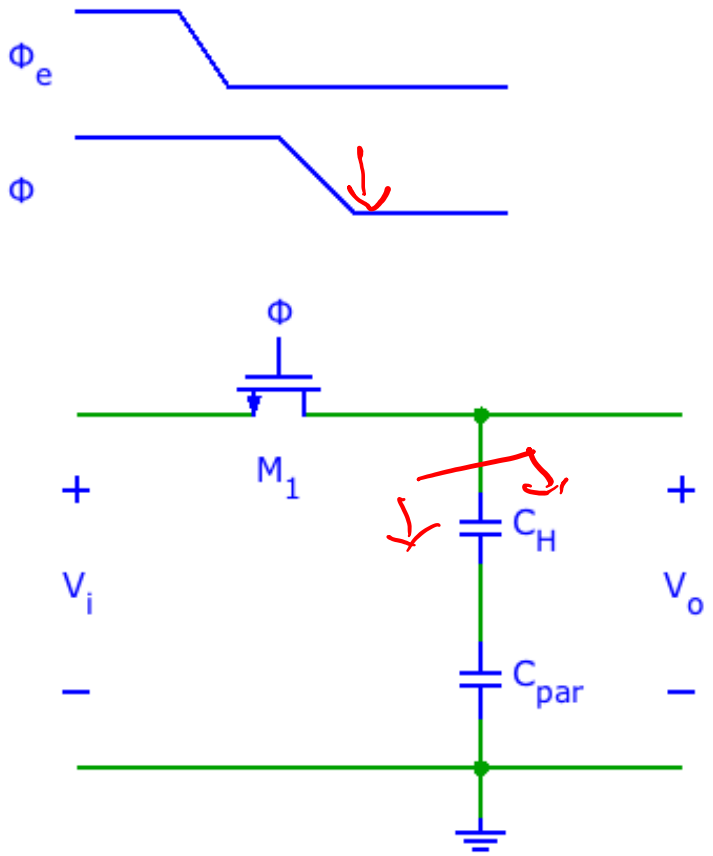


$$\Delta Q_2 = \frac{1}{2} W L C_{ox} \cdot (\Phi_1 - V_{TN})$$

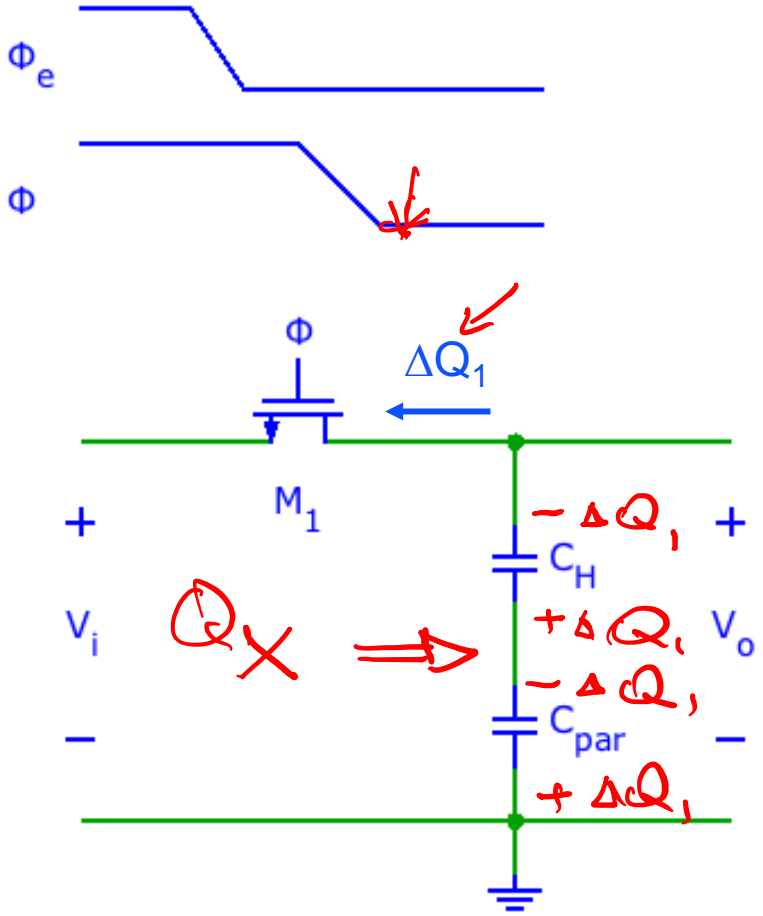
$$\neq f(V_i)$$

$$V_o = V_{in} + \frac{\Delta Q}{C_H}$$

2) Disconnect C_H



Charge at Node X



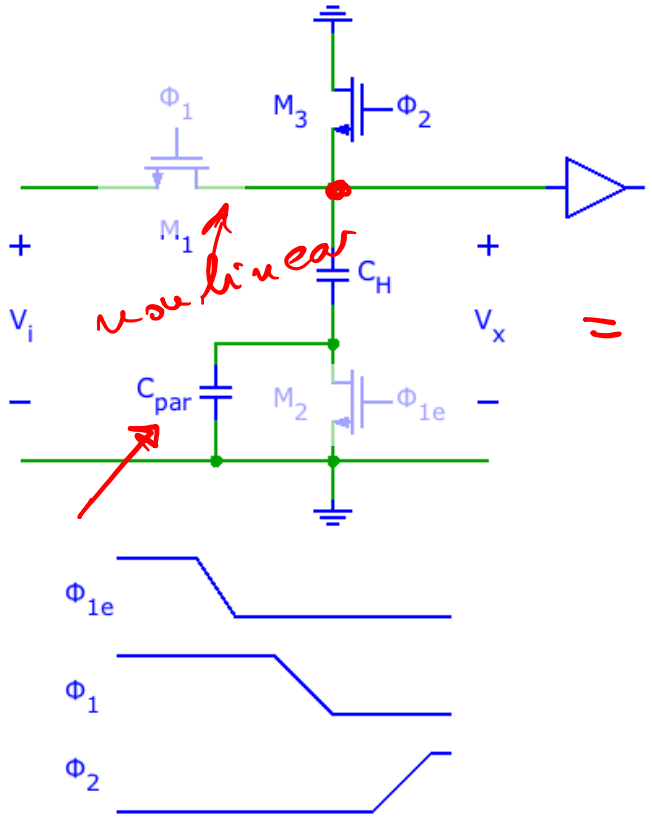
$$Q_x = -C_H \cdot V_i$$

$$+ \Delta Q_1 - \Delta Q_1 \rightarrow 0$$

$$- \Delta Q_2 \rightarrow \text{const.}$$

$$\neq f(V_i)$$

Open-Loop Charge Processing



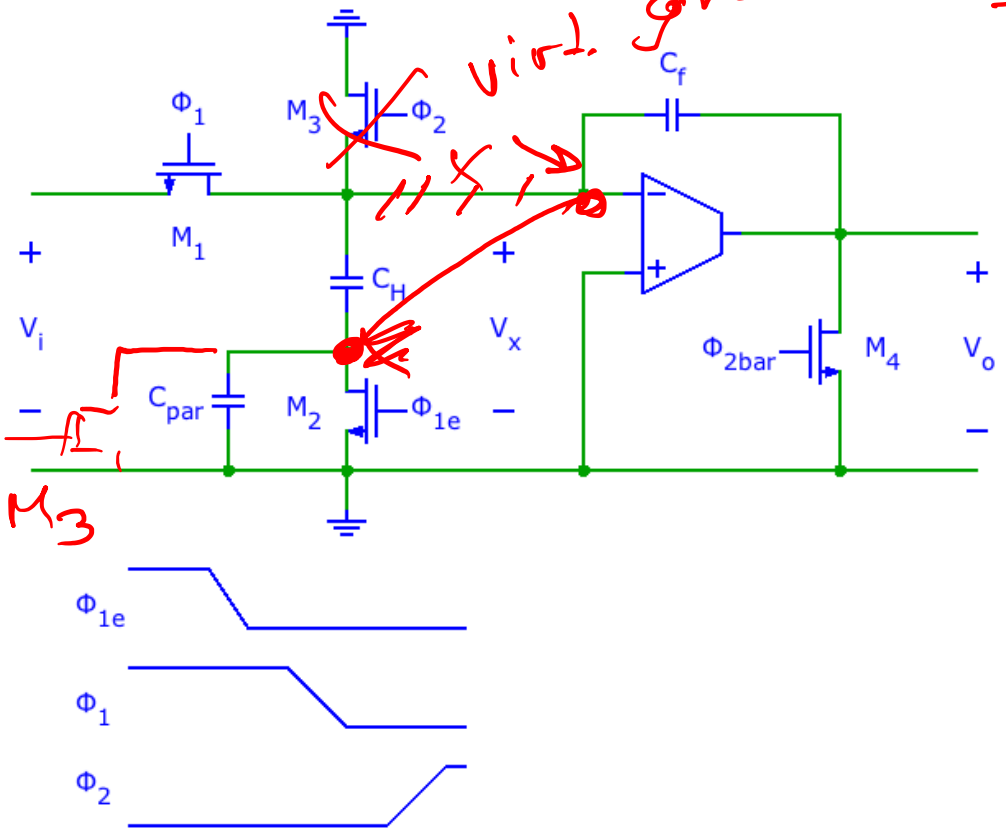
$$\Delta Q_x = -C_H \cdot V_i - \Delta Q_2$$

nonlinear

$$V_x = \frac{\Delta Q_x}{C_H + C_{par}} \neq f(\Delta Q_1)$$

gain error

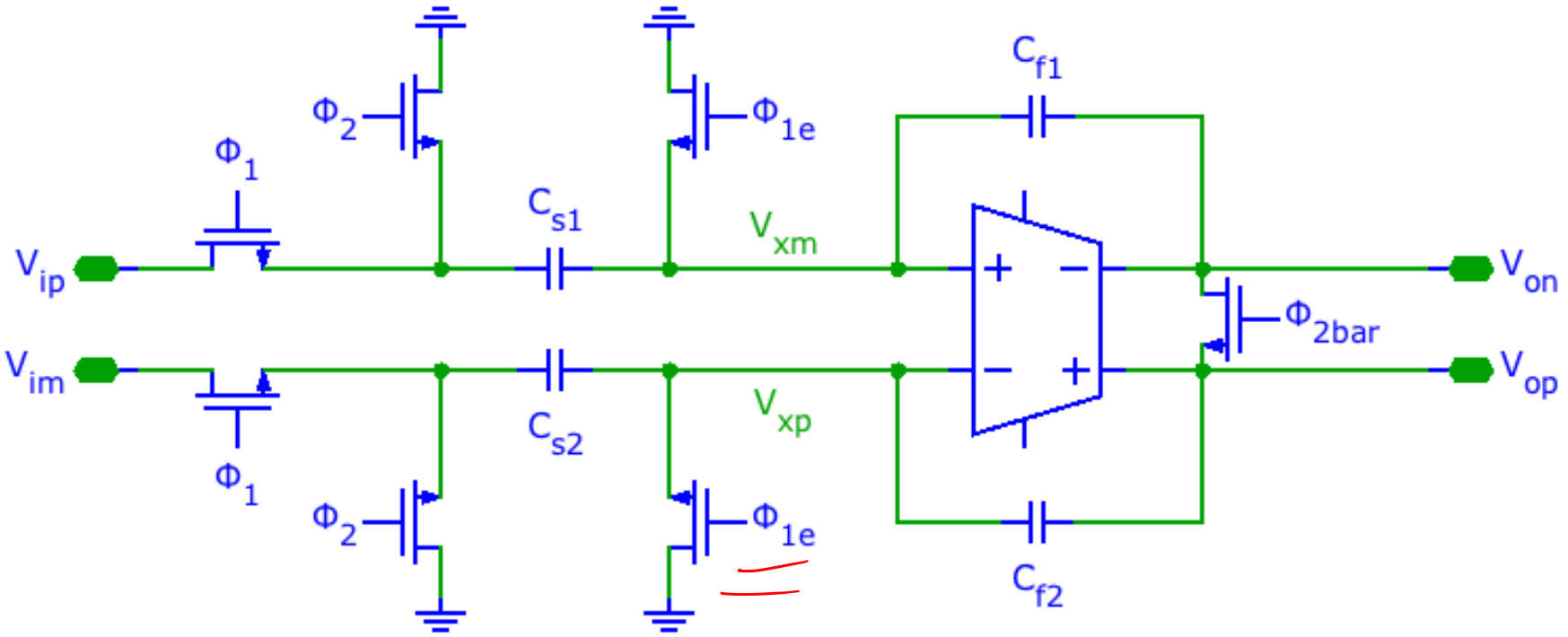
Closed-Loop Charge Processing



Charge Conservation Analysis

$$Q_{x1} = -C \cdot V_{in} - \Delta Q_2 + \alpha C_g \cdot$$

Cancelling the Offset: Fully Differential



$$V_{od} = \frac{C_S}{C_f} \cdot V_{id}$$

$$V_{xc} = \frac{\Delta Q_2 + C_S \cdot V_{oc} - C_S \cdot V_{ic}}{C_S + C_f}$$

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Sampling Network

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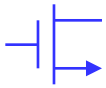
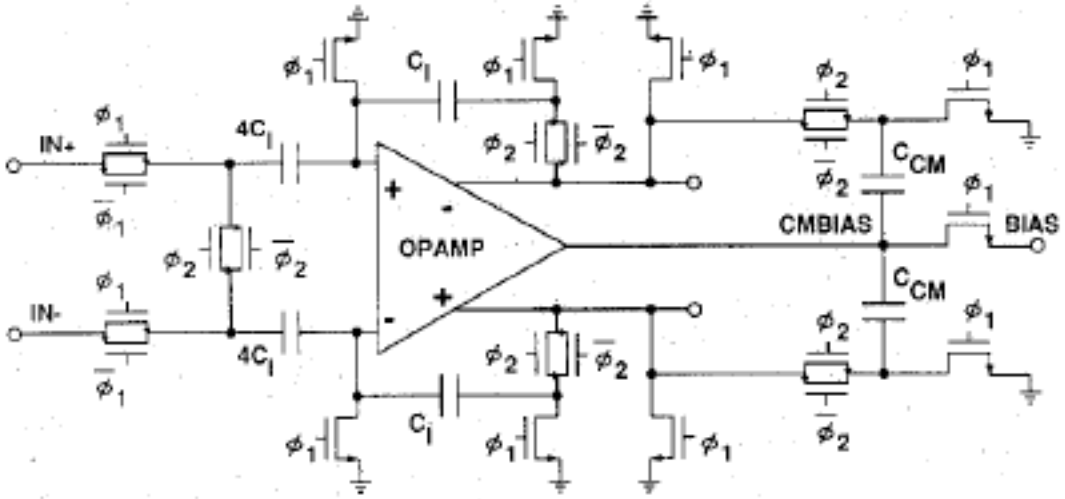
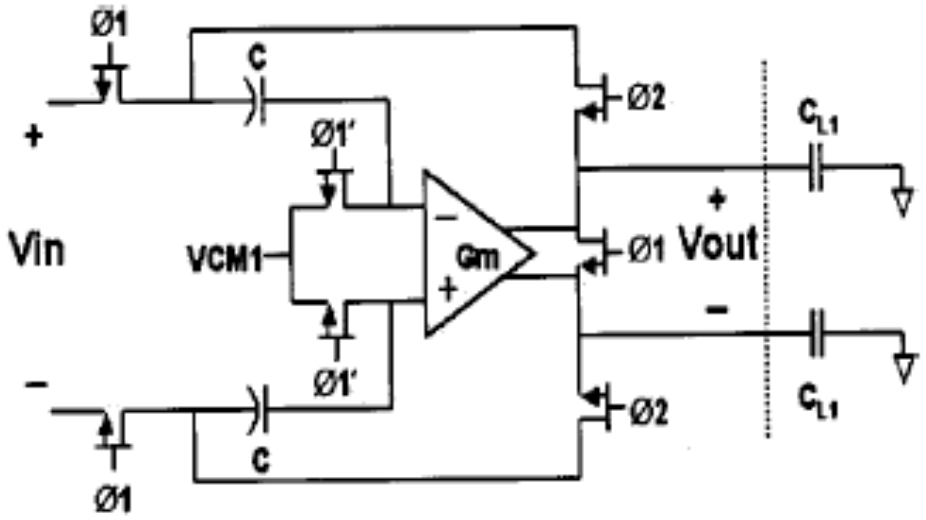


SC Gain with Common-Mode Cancellation



Ref: S. H. Lewis and P. R. Gray, “A pipelined 5 MSample/s 9-bit analog-to-digital converter,” IEEE JSSC Dec 1987, pp. 954-61.

Flip-Around T/H



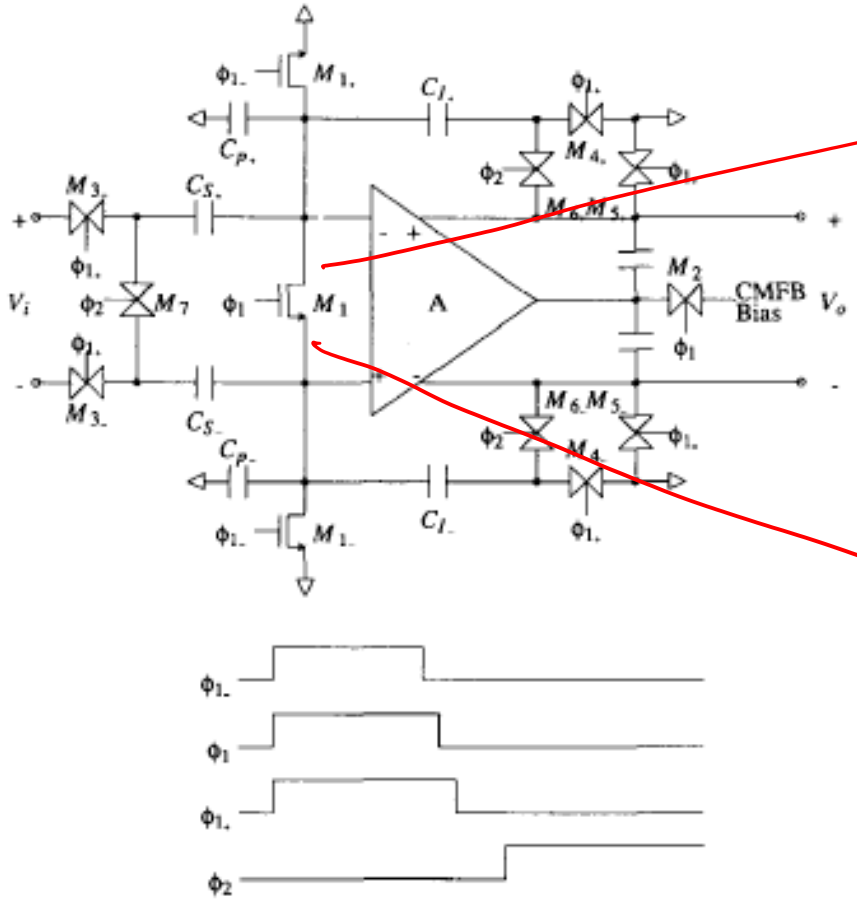
Ref: W. Yang et al, "A 3-V 340-mW 14-b 75-MSample/s CMOS ADC with 85-dB SFDR at Nyquist input," IEEE JSSC Dec 2001, pp. 1931-36.

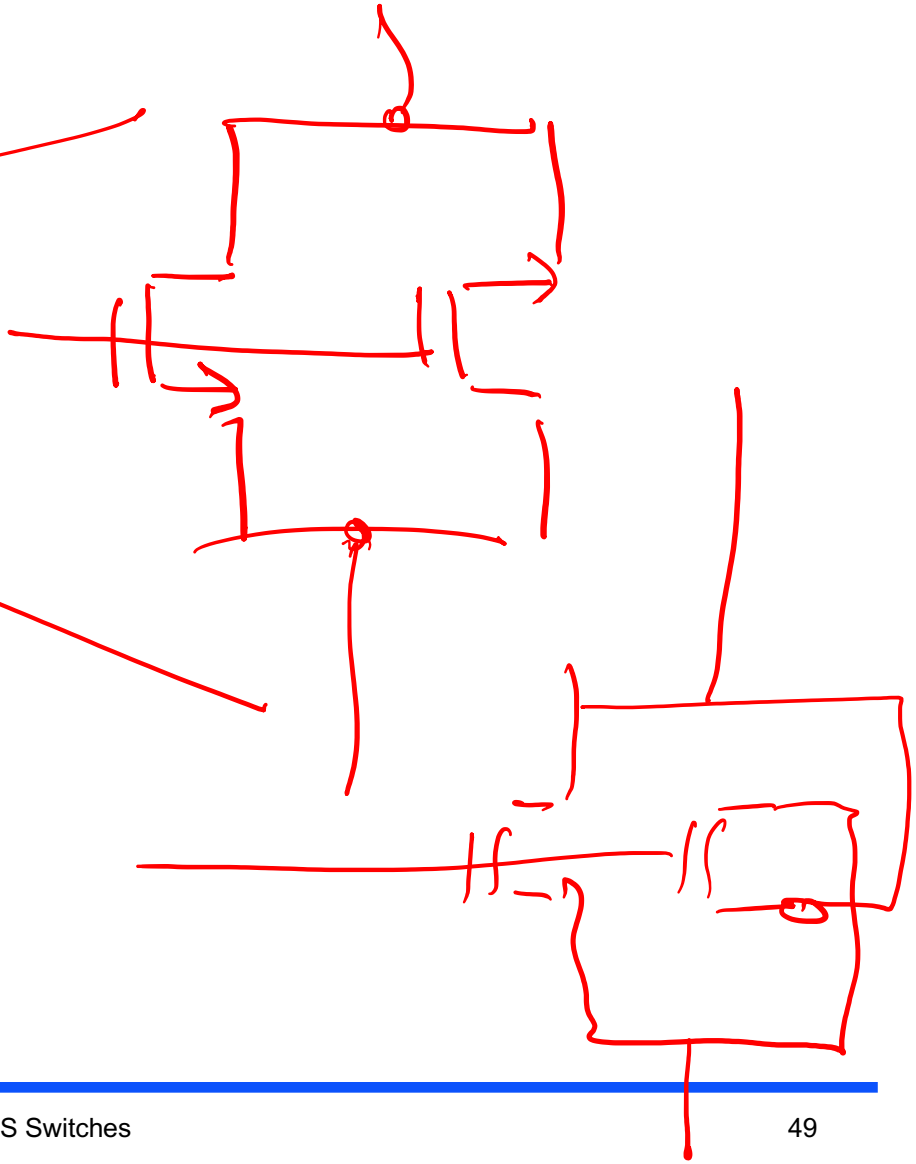
+ β larger

− gain = 1

− Vic

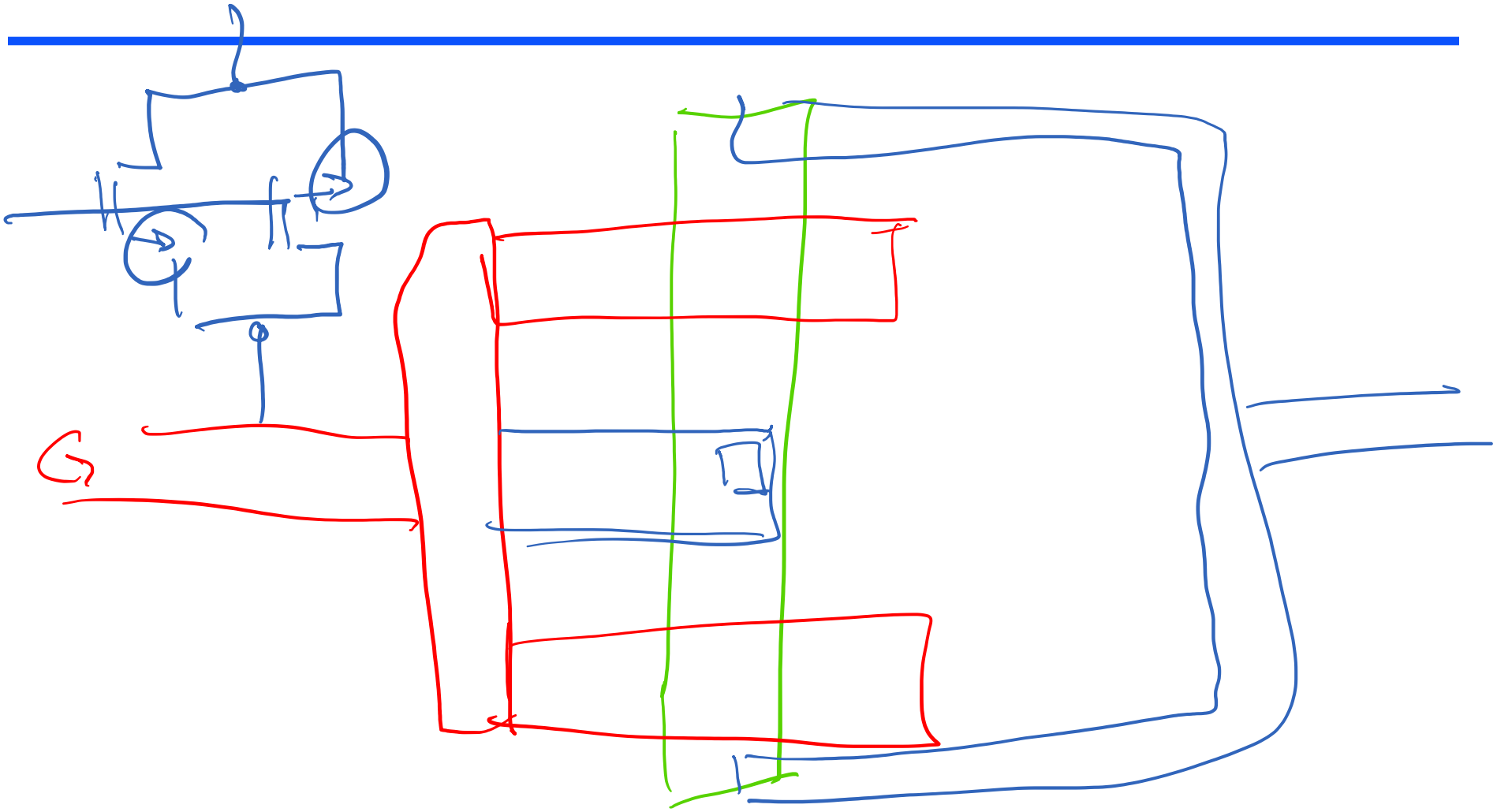
Sampling Network Design





Ref: Y.-M. Lin et al., "A 13-b 2.5-MHz self-calibrated pipelined A/D converter in 3-um CMOS," IEEE JSSC April 1991, pp. 628-36.

Realization of Shorting Switch



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Capacitors

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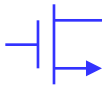
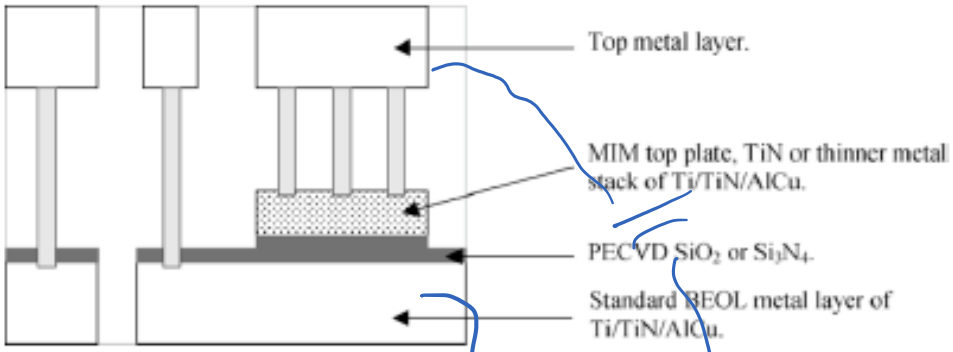
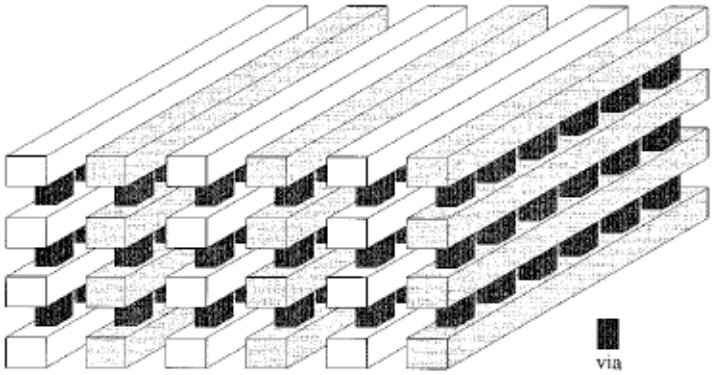


Capacitors

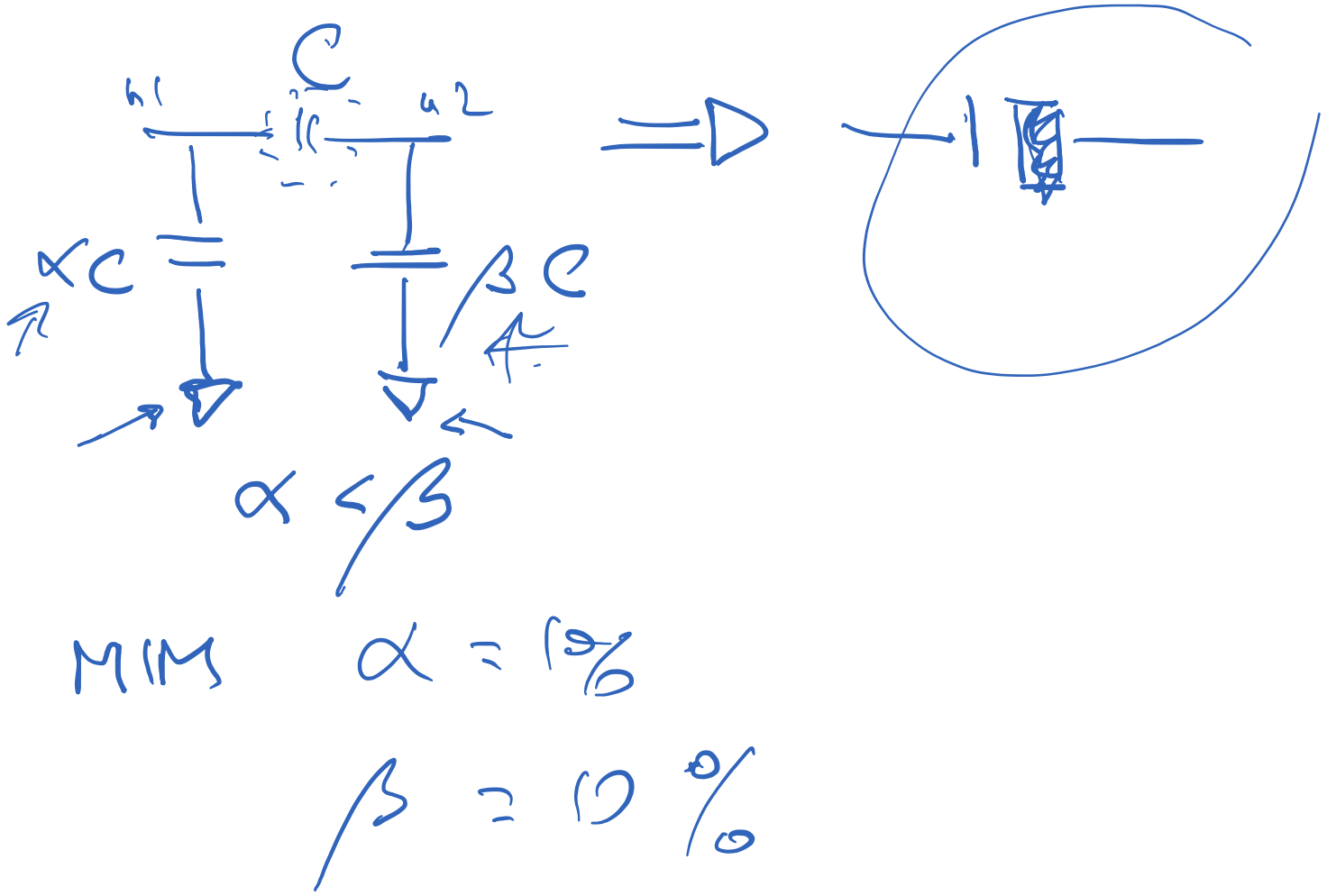


Ref: C. H. Ng et al, "MIM capacitor integration for mixed-signal/RF applications," IEEE Trans ED, July 2005, pp. 1399-1409.



Ref: R. Aparicio et al, "Capacity Limits and Matching Properties of Integrated Capacitors," IEEE JSSC, March 2002, pp. 384-93.

Capacitor Top and Bottom Parasitics



Connection of Capacitors